A Switched-Capacitor and Series-Resonant Hybrid MHz DCX in Data Center Applications

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***Abstract*—In the front-end of two-stage voltage regulator modules in 48V-based data centers, a dc transformer (DCX) is required to convert the 48V bus to an intermediate voltage with a fixed buck ratio. In this paper, we present a novel switched-capacitor and series-resonant hybrid DCX specifically for this application. The proposed DCX combines a 2:1 resonant switched-capacitor cell with a series-resonant converter, enabling a conversion ratio of 4*n*:1 with an *n*:1 transformer. It demonstrates excellent soft-charging and soft-switching performances, effectively mitigating the switching loss. Furthermore, zero voltage switching does not rely on the transformer's magnetizing current. Therefore, the magnetizing inductance can be optimized to improve the efficiency and to facilitate a simplified magnetic design. Theoretical analysis, design considerations, and topology comparison are provided to showcase the advantages of the proposed topology. A 1 MHz, 300 W-rated, 48V to 12V converter prototype is designed and tested. Experimental results well validate the concept with a 97.23% peak efficiency.**

***Index Terms*—Data center, dc transformer, magnetic integration, series resonant converter, switched-capacitor.**

I. Introduction

DATA center has emerged as a critical infrastructure supporting the seamless operation of the digital era [1]. At the load point of data center, the power requirements for high-performance processors are rapidly increasing, characterized by high current (>200A/module) and low logic voltage (<1.8V) [2]. Consequently, the conventional power architecture based on a 12V bus is no longer sufficient. To tackle this challenge, a new generation 48V bus architecture has been proposed [3], [4], as illustrated in Fig. 1(a). This high-voltage architecture offers significant improvements in overall efficiency by reducing bus-bar conduction losses and minimizing the number of power conversion stages.

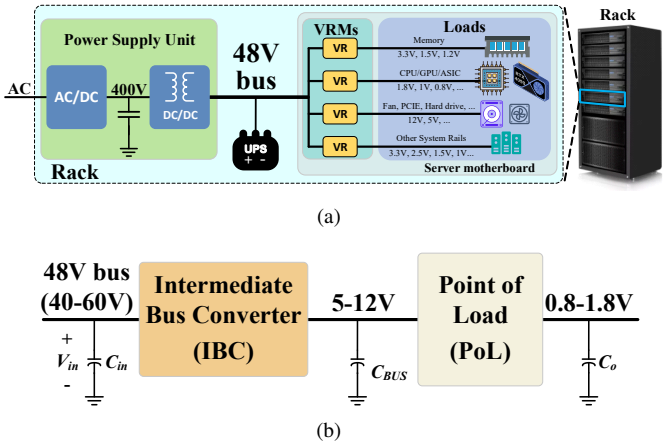

Fig. 1. (a) Emerging 48 V bus power architecture in data center; (b) Two-stage VRM structure.

Meanwhile, the adoption of a 48V architecture brings forth new challenges in achieving optimal design for voltage regulator modules (VRMs). Existing research on 48V VRMs can be classified into two categories: single-stage and two-stage solutions [5]. Although single-stage structure has the potential to achieve higher efficiency and power density, it necessitates complex topologies and control methods to achieve the high step-down ratio. On the other hand, two-stage approach remains prevalent due to its superior deployment flexibility and transient performance [6]. As illustrated in Fig. 1(b), two-stage structure comprises an intermediate bus converter (IBC) followed by a point-of-load (PoL) converter. The IBC converts the bus voltage (40V-60V) to an intermediate voltage (5V-12V). Typically, the IBC operates in an unregulated manner, functioning as a dc transformer (DCX). The research focus for the DCX is compactness, high efficiency, and high-power capability.

State-of-the-art IBCs can be categorized into switched-capacitor-based solutions and transformer-based solutions [5]. Among them, switched capacitor converters (SCCs) emerge as promising candidates for DCX. The utilization of capacitors for energy transfer in SCCs eliminates the need for bulky magnetic components [7]. This results in improved efficiency and compactness due to the higher energy density of capacitors compared with inductors [8]. Furthermore, the concept of resonant SCCs has been introduced by incorporating small inductors into the SCC design. This integration helps eliminate

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charge redistribution losses without obviously compromising power density. An optimized topology known as the switched-tank converter (STC) [6], [9], [10] demonstrates good potential in achieving exceptional power density and efficiency. However, SCCs encounter challenges such as component consistency and large components count [6] when aiming for high voltage conversion ratios. These challenges increase hardware cost and limit scalability.

Alternatively, transformer-based converters offer the advantage of handling high voltage conversion ratios with fewer components, achieved by tuning the turns ratio of the transformer. Among these options, *LLC* DCX [11]–[13] has gained popularity, primarily due to its ability to achieve zero-voltage-switching (ZVS) during the turning on of primary-side MOSFETs and zero-current-switching (ZCS) during the turning off of secondary-side diodes. In order to further enhance the performance of the *LLC* DCX, various techniques have been proposed [14]–[17], including gallium nitride (GaN) based MHz operation, optimization of the intermediate bus voltage, and improved transformer design.

Optimized transformer design is crucial for achieving high efficiency and power density in the *LLC* DCX. Transformer's turns ratio and primary-side structure should be designed synergistically. In general, reducing the turns ratio and the number of primary turns can effectively reduce both winding losses and transformer volume [18], [19]. However, it is important to note that the turns ratio is inversely proportional to the primary switch current stress. Consequently, full-bridge (FB) structure offers lower current stresses on the primary switches but results in an increased turns ratio and primary turns. On the other hand, half-bridge (HB) structure exhibits a smaller turns ratio and fewer primary turns, but current stresses of primary switches are doubled.

Furthermore, the presence of circulating current in the transformer [20], [21] poses challenges not only in magnetic design but also in limiting overall efficiency, particularly at light load. In conventional *LLC* designs, it is crucial to maintain an appropriate magnetizing current in the transformer, ensuring the soft-switching of the primary-side switches [22]. Meanwhile, constraining the magnetizing current can reduce component current stress and conduction loss. Consequently, various modulation schemes and modified primary structures are proposed [23], [24] to restrain the circulating current in the transformer. However, the complex control strategies often come at the cost of sacrificed DCX performance.

To address the aforementioned issues, a hybrid DCX topology is proposed and depicted in Fig. 2. The proposed DCX combines resonant switched-capacitor (SC) cell with series-resonant converter (*SRC*). It retains the advantages of both techniques while mitigating certain limitations. Firstly, it enables a 4*n*:1 voltage conversion ratio with an *n*:1 transformer. Secondly, it reduces the voltage stress on primary switches to half of that in conventional full-bridge and half-bridge *LLC* designs, while maintaining equivalent current stresses as the half-bridge *LLC* at a lower turns ratio. Additionally, a common half-bridge structure is shared between the SC and *SRC* modules. Consequently, all primary switches can achieve ZVS by utilizing the resonant current in the SC's resonant tank. This

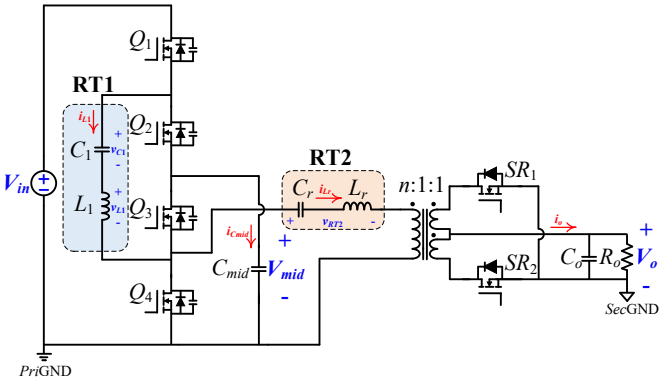


Fig. 2. The schematic of proposed hybrid SCSRC DCX.

feature eliminates the need for the transformer's magnetizing current to realize the ZVS. Thus, the magnetizing inductance can be optimized to restrain the circulating current. Moreover, the switching frequency can be tuned to the resonant frequency of the resonant tank in the series-resonant module to achieve an optimal operation.

II. Operation Principles

The schematic of the proposed hybrid DCX with 4*n*:1 conversion ratio is illustrated in Fig. 2. It combines a 2:1 resonant switched-capacitor cell and a series-resonant converter. The switched-capacitor cell is composed of LC resonant tank 1 (RT1, L_1 and C_1), a non-resonant capacitor C_{mid} and a stacked-bridge ($Q_1 - Q_4$). Q_3 and Q_4 are reused as the input half-bridge of the *SRC*. The *SRC* also consists of LC resonant tank 2 (RT2, L_r and C_r), *n*:1:1 center-tapped transformer, and two synchronous rectifying (SR) switches. The positive current direction and voltage polarity are denoted in Fig. 2.

There are two pairs of complementary gate signals with 50% duty cycle neglecting dead time: Q_1 and Q_2 are one pair, while Q_2 and Q_4 are the other pair. The switching frequency is tuned to the resonant frequency of RT2, ensuring optimal efficiency for *SRC*. To guarantee ZVS of all primary switches, the resonant frequency of RT1 is designed to be slightly lower than switching frequency, allowing sufficient energy storage in L_1 during the switching transition. Additionally, a small phase-shift is inserted between two pairs of gate signals [25]. The phase-shift is set to the minimum required deadband of ZVS. The proposed DCX maintains a nominal voltage conversion ratio of $V_{in} : V_o = 4n : 1$.

To provide a clear and intuitive understanding of the operational principle of the proposed converter, several assumptions are made to simplify the analysis:

1. All parasitic components, except those indicated in the schematic, are considered negligible. Additionally, the output parasitic capacitance C_{oss} of the primary switches is assumed to be identical and linear.
2. The on-state resistance of switches are all $R_{ds,on}$, and the forward voltage drop across the body diode is neglected.
3. The capacitance values of C_{mid} and C_o are assumed to be sufficiently large, and both V_{mid} and V_o can be considered constant at any given time.

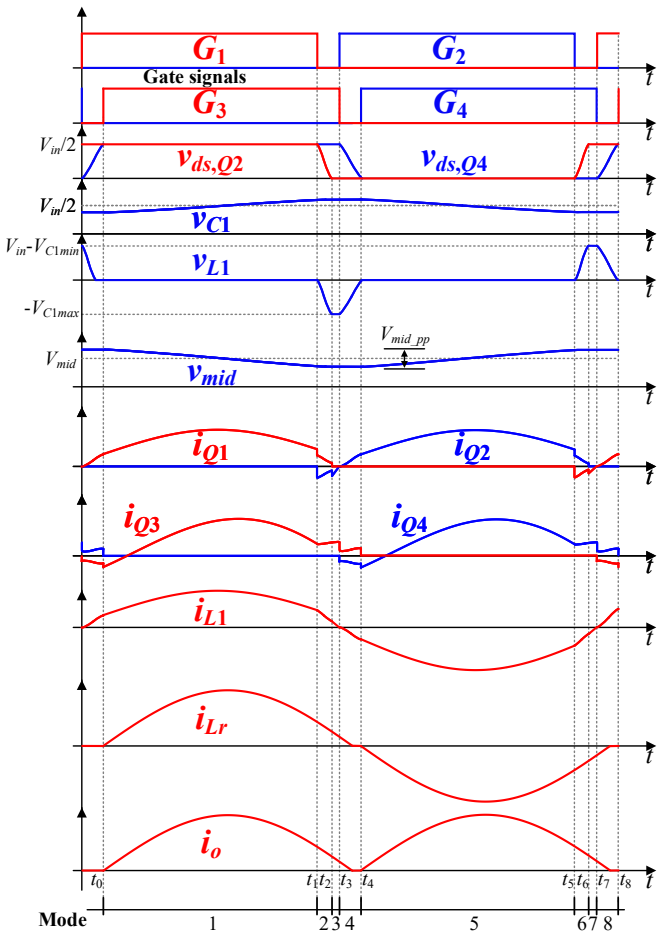


Fig. 3. Ideal switching waveforms of the proposed converter at steady-state.

4. The transformer is assumed to be ideal, with an n:1:1 turns ratio.

The circuit operation can be divided into eight modes, and the key waveforms are depicted in Fig. 3. The waveforms include G_{1-4}, which represent the gate signals of Q_{1-4}, $v_{ds,Q2}$ and $v_{ds,Q4}$ representing the drain-to-source voltages of Q_2 and Q_4, v_{C1} indicating the voltage across C_1, and v_{L1} and i_{L1} representing the voltage and resonant current of L_1. The voltage across C_{mid} is indicated as v_{mid} where V_{mid_pp} represents the the peak-to-peak ripple voltage of C_{mid}. Furthermore, i_{Q1-Q4} represents the current flowing through Q_{1-4}, i_{Lr} represents the resonant currents of L_r, and the output current is denoted as i_o. The corresponding equivalent circuits can be seen in Fig. 4. Due to the operational symmetry, only four modes are detailed for the half switching cycle, ranging from t_0 to t_4.

Mode 1 ($t_0 - t_1$)**:** At $t = t_0$, the C_{oss} of Q_3 and Q_4 have already been fully charged and discharged, resulting in the ZVS turn-on of Q_3. The corresponding equivalent circuit is illustrated in Fig. 4(a). The input voltage source V_{in} charges RT1, RT2, and the output load, while the middle non-resonant capacitor C_{mid} also charges RT2 and the output load. As a result, the current i_{Lr} is the sum of i_{L1} and i_{Cmid}.

Mode 2 ($t_1 - t_2$)**:** At $t = t_1$, Q_1 turns off, and the equivalent circuit is shown in Fig. 4(b). i_{L1} charges and discharges the C_{oss} of Q_1 and Q_2 until the C_{oss} of Q_2 is fully discharged and its body diode conducts, enabling ZVS turn-on of Q_2.

Mode 3 ($t_2 - t_3$)**:** In this interval, the equivalent circuit shown in Fig. 4(c) applies. If i_{L1} has already dropped to zero at $t = t_2$, this interval is bypassed. However, if i_{L1} is positive, Q_3 continues to conduct, while Q_2 is on through its body diode and it can be turned on with ZVS. During this short period, L_1 is in parallel with C_1, and the voltage of C_1 can be considered constant. Consequently, i_{L1} decreases linearly until it drops below zero. The resonant tank 2 in *SRC* cell still operates at a positive half cycle.

Mode 4 ($t_3 - t_4$)**:** This mode is depicted in Fig. 4(d). At $t = t_3$, Q_2 is turned on with ZVS and Q_3 turns off, i_{L1} have reached zero and starts to increase in the opposite direction, while i_{Lr} is still positive. The C_{oss} of Q_3 and Q_4 are then charged and discharged by the difference between i_{L1} and i_{Lr} until the C_{oss} of Q_4 is fully discharged, causing Q_4's body diode to conduct. It enables the ZVS turn-on of Q_4.

Upon conducting a detailed mode analysis, two main modes, Mode 1 and Mode 5, maintain a fixed duty cycle. The remaining operational modes during dead time transition automatically. Consequently, the proposed topology can effectively operate in open-loop control DCX mode with proper dead time. This feature brings the benefits of flexibility and simplicity without requiring complex closed-loop control.

To simplify the analysis, the switching frequency f_s is set equal to the resonant frequency f_r of RT2. Then, i_{Lr} can be considered as a sinusoidal current source, and the expression is given by

$$i_{Lr} = I_p \sin(\omega_r t) \tag{1}$$

where $\omega_r = \dfrac{1}{\sqrt{L_r C_r}}$, and I_p is the amplitude of i_{Lr}.

In Mode 1, applying Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) yields

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} - i_{L1} R_{ds,on} - v_{C1} + i_{Cmid} R_{ds,on} - V_{mid} \\ i_{Lr} = i_{L1} + i_{Cmid} \end{cases} . \tag{2}$$

Solving Eqs. 2 gives

$$\begin{aligned} i_{L1}(t) =& e^{-\alpha t}\{K_1 \cos(\omega_d t) + K_2 \sin(\omega_d t)\} \\ &+ K_3 \cos(\omega_r t) + K_4 \sin(\omega_r t) \end{aligned} \tag{3}$$

where

$$\begin{cases} K_1 = i_{L1}(0) - K_3 \\ K_2 = \dfrac{v_{L1}(0) + \alpha L_1 K_1 - \omega_r L_1 K_4}{\omega_d L_1} \\ K_3 = -\dfrac{\alpha I_p \omega_r \omega_e}{\omega_e^4 + 4\alpha\omega_r^2} \\ K_4 = \dfrac{2\alpha^2 I_p \omega_r^2}{\omega_e^4 + 4\alpha\omega_r^2} \\ \alpha = \dfrac{R_{ds,on}}{L_1} \\ \omega_1 = 1/\sqrt{L_1 C_1} \\ \omega_r = 1/\sqrt{L_r C_r} \\ \omega_d = \sqrt{\omega_1^2 - \alpha^2} \\ \omega_e = \sqrt{\omega_r^2 - \omega_1^2} \end{cases} . \tag{4}$$

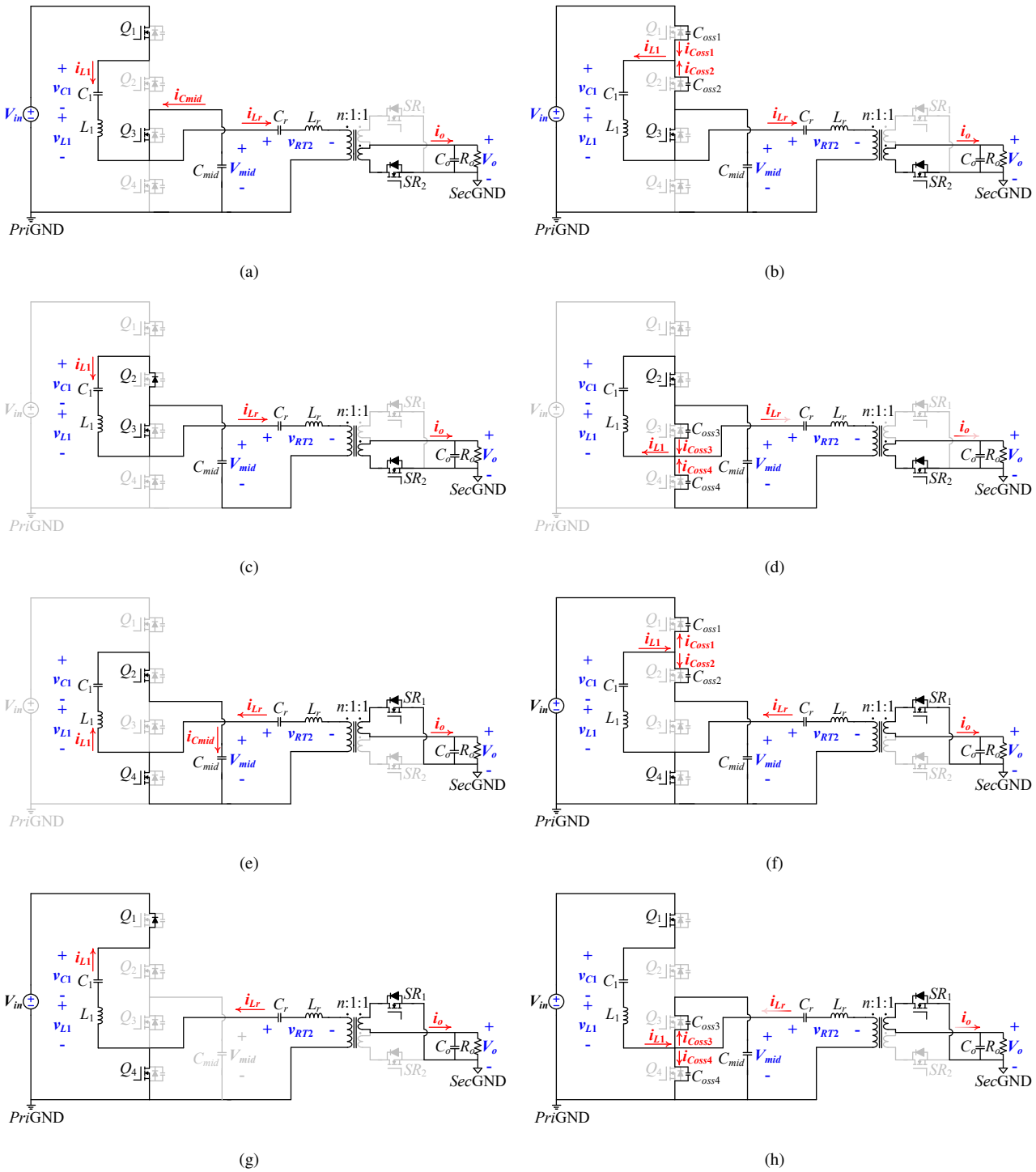


Fig. 4. Equivalent circuits of the proposed converter: (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.

In Mode 5, the KVL and KCL equations are combined and represented as

$$L_1\frac{di_{L1}}{dt} = V_{mid} - i_{L1}R_{ds,on} - v_{C1} - (i_{Lr} - i_{L1})R_{ds,on}. \quad (5)$$

Then i_{L1} can be expressed as,

$$i_{L1}(t) = K_5\cos(\omega_1 t) + K_6\sin(\omega_1 t) + K_7\cos(\omega_r t) \quad (6)$$

where

$$\begin{cases} K_5 = a\cos(\beta\pi) - b\sin(\beta\pi) \\ K_6 = b\cos(\beta\pi) + a\sin(\beta\pi) \\ K_7 = -\dfrac{\alpha I_p \omega_r}{\omega_e^2} \\ a = i_{L1}(\frac{\pi}{\omega_r}) - K_7 \\ b = \dfrac{v_{L1}(\pi/\omega_r)}{\omega_1 L_1} \\ \beta = \omega_1/\omega_r \end{cases}. \quad (7)$$

III. Critical Analysis

A. ZVS Analysis

For the upper-bridge switches $Q_{1,2}$, ZVS can be achieved when the energy stored in L_1 is sufficient to fully charge and discharge the C_{oss} of $Q_{1,2}$ during the dead time. Mathematically, this condition can be expressed by the inequality:

$$\frac{1}{2}L_1 i_{L1\_dt}^2 \geq C_{oss}V_{ds}^2 \tag{8}$$

where i_{L1_dt} is the current flowing through L_1 at the beginning of the dead time, and V_{ds} is the drain-to-source voltage of switch. It is important to note that in the proposed converter, all primary-side switches have identical C_{oss} and V_{ds}, with V_{ds} being equal to $V_{in}/2$.

For the lower-bridge switches $Q_{3,4}$, the ZVS processes correspond to the modes 4 and 8. At the beginning of these two modes, i_{L1} must be zero and then charges and discharges the C_{oss} of $Q_{3,4}$ with the opposite current direction to the previous mode.

During one switching cycle, there are four deadbands, which correspond to Mode 2, Mode 4, Mode 6, and Mode 8. The equivalent circuits are plotted in Fig. 4. The minimum dead time t_d is determined by the time required to charge and discharge the C_{oss} of the switches. For estimating t_d, Mode 4 with $i_{Lr} = 0$ is used as an example and the on-state resistance $R_{ds,on}$ of primary-side switches is neglected. In this case, v_{C1} is assumed to remain constant during the dead time and is approximately equal to V_{mid}. The state equations can be expressed as follows:

$$\begin{cases} v_{C1} + v_{L1} + v_{ds,Q4} = V_{mid} \\ v_{L1} = L_1 \dfrac{di_{L1}}{dt} \\ i_{L1} = 2C_{oss}\dfrac{dv_{ds,Q4}}{dt} \end{cases} \tag{9}$$

with the initial state

$$\begin{cases} v_{C1} = V_{mid} \\ v_{ds,Q4}(t_3) = \dfrac{V_{in}}{2} \\ i_{L1}(t_3) = 0 \end{cases}. \tag{10}$$

Thus, the expressions of $v_{ds,Q4}$ and i_{L1} can be calculated as:

$$\begin{cases} v_{ds,Q4}(t) = \dfrac{V_{in}}{2}cos(\omega_0(t-t_3)) \\ i_{L1}(t) = -\dfrac{V_{in}}{2Z_0}sin(\omega_0(t-t_3)) \end{cases} \tag{11}$$

where $\omega_0 = \dfrac{1}{\sqrt{2C_{oss}L_1}}$, and $Z_0 = \sqrt{\dfrac{L_1}{2C_{oss}}}$.

Since $v_{ds,Q3} + v_{ds,Q4} = V_{mid} = \dfrac{V_{in}}{2}$, two trajectories during Mode 4 can be derived:

$$\begin{cases} (v_{ds,Q4}(t))^2 + (i_{L1}(t)Z_0)^2 = (\dfrac{V_{in}}{2})^2 \\ (v_{ds,Q3}(t) - \dfrac{V_{in}}{2})^2 + (i_{L1}(t)Z_0)^2 = (\dfrac{V_{in}}{2})^2 \end{cases}. \tag{12}$$

Therefore, the complete trajectories of i_{L1} with respect to $v_{ds,Q3}$ and $v_{ds,Q4}$ are illustrated in Fig. 5. The minimum dead time t_d necessary to achieve ZVS must satisfy the following inequality:

$$t_d \geq \frac{\pi/2}{\omega_0} = \frac{\pi}{2}\sqrt{2C_{oss}L_1}. \tag{13}$$

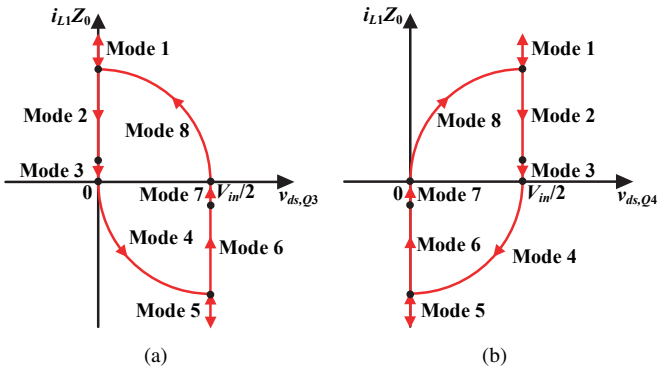


Fig. 5. Trajectory: (a) i_{L1}-$v_{ds,Q3}$; (b) i_{L1}-$v_{ds,Q4}$.

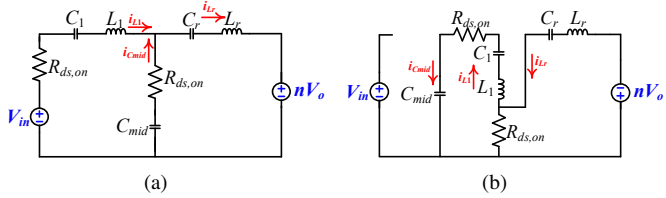


Fig. 6. Simplified equivalent circuits: (a) Mode 1. (b) Mode 5.

B. Electrical Rating Analysis

The electrical rating not only determines the component selection, but also affects the power loss of converter [26]. To simplify the analysis, the dead time during switching transition is neglected. The further simplified equivalent circuits are shown in Fig. 6.

The switch voltage rating is determined by the voltage across the capacitors. In the 2:1 SC part, both the DC components of the voltages V_{mid} and v_{RT1} are equal to $V_{in}/2$, which results in equivalent voltage stresses of $V_{in}/2$ on Q_1 to Q_4. The current stress on the switches depends on the currents flowing through the two resonant tanks, namely i_{L1} and i_{Lr}. The relationships between these currents are satisfied as follows:

$$\begin{cases} i_{Cmid} = i_{Lr} - i_{L1}, & \text{in Mode 1} \\ i_{Cmid} = i_{L1}, & \text{in Mode 5} \end{cases}. \tag{14}$$

As the durations of Mode 1 and Mode 5 are both 50% of the switching period, i_{L1} and i_{Cmid} are both equal to $i_{Lr}/2$. In Mode 1, Q_1 carries i_{L1}, while Q_3 carries i_{Cmid}. In Mode 5, Q_3 carries i_{L1}, and Q_4 carries $i_{Lr} - i_{L1}$. Therefore, the current stresses on Q_1 to Q_4 can be considered $i_{Lr}/2$.

C. Tolerance of Resonant Components

In the theoretical analysis, the *SRC* cell can achieve optimal efficiency as long as the switching frequency is matched to

the resonant frequency. However, in practice, once there is a small error in the resonant parameters, the match will be lost. Thus, ensuring consistent resonant parameters during large-scale production poses a significant challenge.

One of the primary causes of mismatch in resonant parameters is the capacitance degradation under dc bias. To mitigate this issue, selecting the resonant capacitor with class I material (e.g. C0G) is advisable, as it exhibits minimal capacitance variation under dc bias.

Furthermore, mismatches in resonant inductors mainly attribute to stray inductors in the loop. To address this issue, it is crucial to optimize printed-circuit-board (PCB) layout to minimize the parasitic inductance. Additionally, adding a deadband during the switching transition can reset resonant currents [9], ensuring the current reaches zero before entering the next mode, even if there is a resonant parameter mismatch. For the proposed SCSRC, Mode 3 is an extra mode to reset i_{L1}, while i_{Lr} is reset during Mode 4.

D. Tolerance of Primary Switches

Assuming the C_{oss} of primary switches are different, the charging and discharging processes of $Q_{1,2}$ are examined to analyze the primary switch C_{oss}'s effect on the C_{mid}'s charge balance. The corresponding modes are Mode 2 and Mode 6, as shown in Fig. 4.

In Mode 2, the charging and discharging process of $C_{oss1,2}$ can be expressed as

$$\begin{cases} Q_{Coss1} = \int i_{Coss1}\, dt = C_{oss1}(V_{in} - V_{mid}) \\ Q_{Coss2} = -\int i_{Coss2}\, dt = -C_{oss2}(V_{in} - V_{mid}) \\ C_{oss1} \neq C_{oss2} \Rightarrow Q_{oss1} + Q_{oss2} \neq 0 \end{cases} \tag{15}$$

where $Q_{Coss1,2}$ are the changed charge of $C_{oss1,2}$, and V_{mid} is the voltage of C_{mid} during Mode 2.

Similarly, the charging and discharging process of $C_{oss1,2}$ in Mode 6 can be expressed as

$$\begin{cases} Q'_{Coss1} = -\int i_{Coss1}\, dt = -C_{oss1}(V_{in} - V'_{mid}) \\ Q'_{Coss2} = \int i_{Coss2}\, dt = C_{oss2}(V_{in} - V'_{mid}) \\ C_{oss1} \neq C_{oss2} \Rightarrow Q'_{oss1} + Q'_{oss2} \neq 0 \end{cases} \tag{16}$$

where $Q'_{Coss1,2}$ are the changed charge of $C_{oss1,2}$, and V'_{mid} is the voltage of C_{mid} during Mode 6.

When the converter is in steady state, the capacitor charge balance must be enforced. Thus, in a steady-state switching cycle,

$$\begin{cases} Q_{Coss1} + Q'_{Coss1} = 0 \\ Q_{Coss2} + Q'_{Coss2} = 0 \end{cases} \Rightarrow V_{mid} = V'_{mid}. \tag{17}$$

Consequently, the charge balance of C_{mid} remains unaffected even if there are differences in primary switches C_{oss}. As a result, the voltage balance control for V_{mid} is unnecessary to handle the tolerance of primary switches.

E. Selection of C_{mid}

According to the analysis in Section II, the middle non-resonant capacitor C_{mid} provides about half of the output energy in a steady-state switching period, and then the energy requirement of C_{mid} can be calculated as,

$$\begin{aligned} W =& \frac{P_o}{2f_s} \\ =& \frac{1}{2}C_{mid}(V_{mid} + \frac{1}{2}V_{mid\_pp})^2 \\ & - \frac{1}{2}C_{mid}(V_{mid} - \frac{1}{2}V_{mid\_pp})^2 \\ =& C_{mid}V_{mid}V_{mid\_pp} \end{aligned} \tag{18}$$

where V_{mid_pp} is the peak-to-peak ripple voltage of C_{mid}, and P_o is the output power.

Therefore, the selection of C_{mid} should comply following constraint,

$$C_{mid} \geq \frac{P_o}{2f_s V_{mid} V_{mid\_pp}}. \tag{19}$$

In practice, C_{mid} is implemented using ceramic capacitors with class II material (eg. X7R, X5R) to reduce the cost. Thus, the capacitance degradation under dc bias should be considered to meet the Eq. (19). Moreover, 1% ripple voltage is preferred to maintain a stable middle voltage.

F. Loss Analysis

For the proposed SCSRC, the dominant losses can be divided into four parts: magnetic loss, semiconductor loss, capacitor loss, and other losses.

1) Magnetic loss: The magnetic components in the proposed converter include a transformer and two resonant inductors. Their loss optimization and estimation are crucial for achieving high efficiency and high power density. To balance efficiency and size, the design process is detailed in Section IV.

2) Semiconductor loss: It consists of both switching loss and conduction loss. When ZVS is lost for certain switches at light load, the switching loss is dominated by the output capacitance loss since i_{L1} is approximately zero at the switching instant. The switching loss P_{sw} can be estimated by

$$P_{sw} = \frac{1}{2}C_{oss}V_{ds}^2 f_s. \tag{20}$$

As the power increases, the converter achieves the ZVS turn-ON for all primary-side MOSFETs and ZCS turn-OFF for secondary-side SRs. Thus, the semiconductor loss primarily attributes to the conduction loss P_{cond} of primary-side MOSFETs and secondary-side SRs,

$$P_{cond} = I_{rms\_sw}^2 R_{on} \tag{21}$$

where I_{rms_sw} and R_{on} represent the root-mean-square (RMS) current flowing through the switches and its on-state resistance, respectively.

3) Capacitor loss: Power loss on ceramic capacitors is also a vital part of the total loss and can be evaluated using their equivalent series resistances (ESR) and RMS currents. To support high current and reduce the ESR, multiple capacitors are paralleled to form a capacitor bank. Then, the capacitor loss P_{cap} can be calculated by

$$P_{cap} = I_{rms\_cap}^2 \frac{R_{cap}}{N_{cap}} \tag{22}$$

where R_{cap} is the ESR of a ceramic capacitor, N_{cap} is the capacitor number in one capacitor bank, and I_{rms_cap} represents the RMS value of current that flows through one capacitor bank.

4) Other losses: High-frequency ac current leads to considerable additional losses due to parasitic resistance in the circuit loop and terminal connections. These losses can be minimized in standardized manufacturing processes by optimizing the current loops.

IV. Magnetic Design

A. Transformer Design

In this study, a planar transformer is selected for operation at 1 MHz switching frequency to achieve a lower magnetic profile and high power density. The secondary side turns number is set to unity to accommodate high load current. Consequently, the primary side turns can be calculated as $N = V_{in}/4V_o = 1$. This leads to the design of a center-tapped transformer with a turns ratio of 1:1:1. The high-frequency magnetic material DMR51W, provided by DMEGC is selected. To constrain the core loss, it is important to ensure that the maximum magnetic flux density B_m does not exceed 100 mT, as indicated by the loss characteristics specified in the datasheet. Therefore, a loss density P_V of 600 mW/cm^3 is considered acceptable with even flux density, which corresponds to a maximum magnetic flux density of approximately 73 mT at 1 MHz. However, due to potential uneven flux distribution leading to sharply increased core loss, a peak flux density of 50 mT is selected as a conservative parameter for core size design. The effective cross-sectional area of the core can be calculated using the formula:

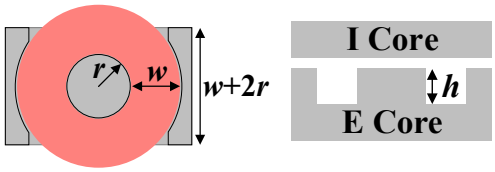
$$A_e = \frac{D_{SRC} V_o}{2 f_s N B_m}. \tag{23}$$

Here, D_{SRC} represents the duty cycle of the *SRC* cell, typically set to 50%.

For the proposed SCSRC, the resonant current in the SC's resonant tank provides the ZVS conditions for all primary switches, and then the transformer's magnetizing current is not necessary for ZVS process of primary switches. Consequently, in the practical design, the magnetizing inductance can be maximized without air gap to restrain the circulating current.

An EI core with customized size is selected to design the planar transformer, and the core and winding structure are illustrated in Fig. 7. *r* represents the radius of the center leg, and it depends on the effective cross-sectional area of the core $A_e = \pi r^2$. w is the winding width, and it is used as a variable parameter to optimize the core structure and power loss. h denotes the height of the window area, and it is determined by the thickness of PCB winding. To simplify the design, the side leg of the core can be approximated as a square, and its estimated length multiplied by width is $(w + 2r) \times \frac{A_e}{2(w+2r)}$. Consequently, the core volume can be computed as

$$V_{core} = 2A_e h + 4A_e\{w + r + \frac{A_e}{2(w + 2r)}\}. \tag{24}$$



(a) (b)

Fig. 7. Diagram of core dimensions: (a) Top view; (b) Cross-section view.

The core loss P_{core} can be estimated by the Steinmetz equation,

$$P_{core} = P_V V_{core} = (k B_m^{\alpha} f^{\beta}) V_{core} \tag{25}$$

where the coefficients k, α, β can be obtained from the datasheet of core material.

Taking into account the load current and footprint requirements, the proposed transformer is implemented with a 12-layer PCB winding, and it is assembled by two single 6-layer PCB boards with 1oz copper to control the cost. Six windings are integrated into the main board, and an extra 6-layer board with other windings is mounted on the main board by bare copper pads. The winding arrangement is demonstrated in Fig. 10, where layers 2, 5, 8, and 11 are paralleled to form primary windings, layers 1, 4, 7, 10 are paralleled to form the first set of secondary windings, and layers 3, 6, 9, and 12 are paralleled to form the second set of secondary windings. SRs and capacitors are placed at the terminations on Layer 1 winding, and multiple copper-plated vias are used to connect the paralleled layers. Each layer has one turn, and the primary and secondary windings are perfectly interleaved to reduce the ac losses caused by the proximity effect.

The copper loss P_{copper} of winding is determined by the winding resistance and RMS current. The dc winding resistance can be calculated as

$$R_{dc} = \frac{\rho \cdot 2\pi}{h} \frac{1}{ln(r + w) - ln(r)} \tag{26}$$

where ρ and h are the resistivity and thickness of copper, respectively. The ac winding resistance can be calculated by Dowell's model [27], [28],

$$R_{ac} = R_{dc}\{\Re(M_w) + \frac{m^2 - 1}{3}\Re(D_w)\} \tag{27}$$

with

$$\begin{cases} M_w = \lambda h \coth(\lambda h) \\ D_w = 2\lambda h \tanh(\lambda h/2) \\ \lambda = \sqrt{\frac{j2\pi f_s \mu_0 \eta}{\rho}} \end{cases} \tag{28}$$

where μ_0 is the vacuum permeability, and m is the number of layers in a winding portion. Since the primary and secondary windings are perfectly interleaved, $m = 1$. Moreover, η can be approximately equal to 1 when the window area is fully utilized.

Using the previously discussed core and copper loss models, the total losses and core volume of the transformer are evaluated for various winding widths, denoted by w, as shown in Fig. 9. The blue curves represent the transformer losses,

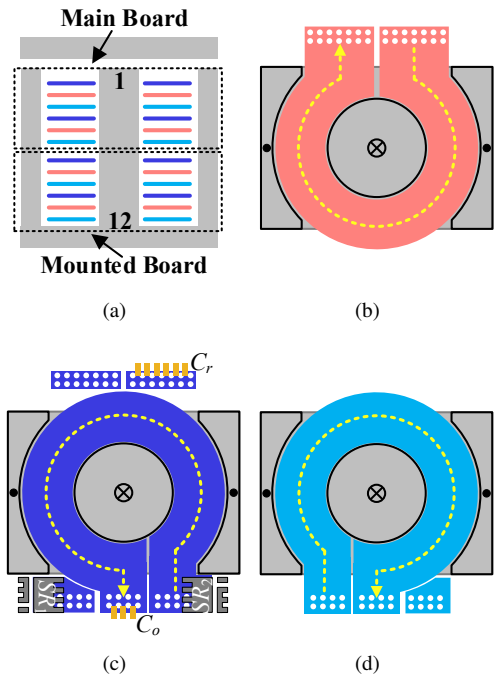


Fig. 8. PCB winding arrangement with perfectly interleaving: (a) 12 layers PCB arrangement. (b) Layers 2, 5, 8, and 11 for primary windings. (c) Layers 1, 4, 7, 10 for the first set of secondary windings (only Layer 1 has the SRs and capacitors). (d) Layers 3, 6, 9, 12 for the second set of secondary windings.

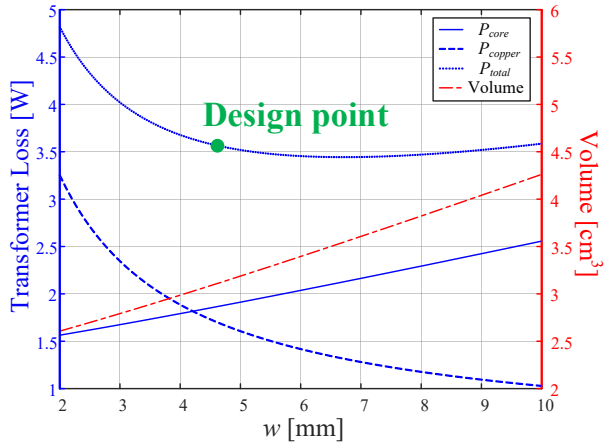


Fig. 9. Transformer loss and core volume with different winding width w.

while the red curve represents the core volume. To strike a balance between efficiency and power density, the optimal design point is determined at a winding width of $w = 4.6$ mm. This design choice achieves an effective tradeoff between the two objectives. The final dimensions of the transformer core is shown in Fig. 10(a).

An ANSYS Maxwell 3D model is developed to analyze and validate the designed core structure of the transformer. As shown in Fig. 10(b), the magnetic flux distribution in the EI core is observed to be symmetric and balanced. While certain regions exhibit flux crowding, the overall distribution remains relatively even. Furthermore, this core structure exhibits a leakage inductance of approximately 15 nH when there is no air gap, which can effectively function as the resonant

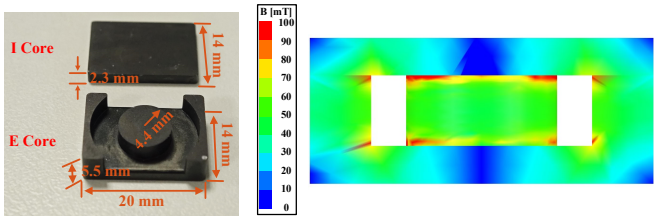


Fig. 10. (a) Dimensions of the designed transformer core. (b) Symmetric and balanced flux distribution of the designed transformer.

inductance for the *SRC* in the MHz operation range. The inclusion of this resonant inductor further enhances the overall power density of the transformer.

B. Inductor Design

Inductor design is crucial for achieving high power density and high efficiency in the proposed DCX. The main targets are minimizing the core loss and copper loss of the inductor while maintaining a low profile and small footprint.

In the proposed SCSRC DCX, a small inductor L_1 is inserted in SC cell to facilitate soft charging of the capacitor and soft switching of the switches. Typically, a 100 nH inductance is preferred, and its volume has minimal impact on the overall power density. Moreover, L_1 is a high-frequency ac inductor with an approximate sinusoidal current, and thus the planar inductor with PCB winding is competitive in efficiency and power density. In this design, the inductance is specifically 120 nH considering the ZVS range.

Compared to a conventional UI structure with a rectangular leg, a URS structure with a cylindrical leg is selected as the inductor core to optimize the winding length. As shown in Fig. 11(a), the dimensions of core is normalized by leg radius r_L and winding width w_L,

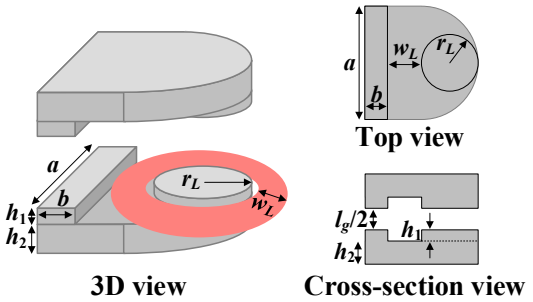
$$\begin{cases} a = 4r_L \\ b = A_L/a = h_2 = 2h_1 \\ A_L = \pi r_L^2 = \frac{L_1 I_{Lp}}{N_L B_m} \\ F_p = a(2(w_L + r_L) + b) \end{cases} \tag{29}$$

where A_L is the cross-sectional area of inductor core, I_{Lp} is the peak current of i_{L1}, N_L is the number of turns, and F_p is the footprint of the inductor.

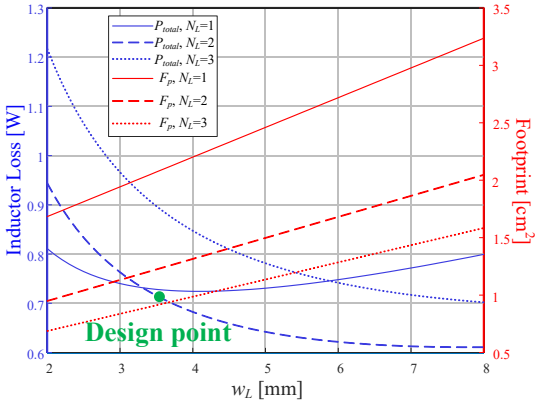
Similar to the transformer design, DMR51W with identical loss density profile is still a suitable core material for inductor design. The analytical model based on the Steinmetz equation and Dowell's model can still be employed to get the total inductor losses. The major difference is that the number of turns N_L is also a variable to optimize the volume and loss. The total losses and footprint of the inductor are plotted for various w_L and N_L, as illustrated in Fig. 11(b). As a result, the designed values are $w_L = 3.5$ mm and $N_L = 2$ to balance the loss and footprint.

Finally, given the targeted L_1, the air gap l_g can be obtained,

$$l_g = R_g \mu_0 A_L = \frac{N_L^2 \mu_0 A_L}{L_1} \tag{30}$$



(a)



(b)

Fig. 11. (a) Dimensions of inductor core. (b) Inductor loss and footprint with different w_L and N_L.

where R_g is the reluctance of air gap.

V. Comparison with Existing Counterparts

A. Topology Comparison

The resonant frequency of conventional *LLC* and *SRC* converter is derived as:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \tag{31}$$

For *LLC*, the input impedance of the resonant tank should be inductive to achieve ZVS for the primary-side switches. Moreover, it is also desirable for the switching frequency f_s to be lower than the resonant frequency f_r, which enables ZCS turning off of SRs. However, the circulating current in transformer increases as f_s decreases, resulting in increased transformer's loss. For a *SRC*, the switching frequency should be greater than the resonant frequency to achieve ZVS. However, the secondary-side SRs lose the ZCS and suffer from high di/dt during the switching transition. For proposed hybrid converter, it can achieve ZVS without relying on the circulating current in the transformer. This unique feature allows the converter to eliminate the transformer's circulating current to optimize the magnetic design and operate at optimal frequency to improve efficiency.

Table I presents a topology comparison among the conventional HB or FB *LLC*, *SRC*, and the proposed topology. The comparison is based on primary switch count, transformer turns ratio, switching frequency, primary switch stresses, and magnetizing current.

TABLE I
Comparison of $4n$:1 Topologies

Topology Structure	*LLC*		*SRC*		Proposed
	HB	FB	HB	FB	
Primary Switch Count	2	4	2	4	4
Turns Ratio	$2n$:1	$4n$:1	$2n$:1	$4n$:1	n:1
Switching Frequency	$f_s < f_r$		$f_s > f_r$		$f_s \approx f_r$
Primary Switches	ZVS		ZVS		ZVS
Secondary SRs	ZCS		Hard Switching		ZCS
Voltage Stress*	2		2		1
Current Stress*	2	1	2	1	2
Magnetizing Current	Large		Small		Small

* It represents the switch stress of primary switches, and its value has been approximated and normalized.

All topologies are designed to achieve a $4n$:1 voltage conversion ratio. As shown, the proposed topology has the smallest turns ratio. In the *LLC* topology, ZVS is achieved by operating at a lower switching frequency than its resonant frequency, utilizing the magnetizing current. On the other hand, the *SRC* topology requires a higher switching frequency than its resonant frequency to achieve ZVS.

In contrast, the proposed topology enables independent implementation of ZVS for the primary switches, regardless of the circulating current in the transformer. This allows for setting the switching frequency at the resonant frequency of RT2 while eliminating the circulating current in the transformer. Additionally, the proposed topology demonstrates the lowest voltage stress on the primary switches and maintains an identical current stress as the HB structure, with a lower turns ratio. Therefore, lower voltage-rating switches with lower costs and better figure-of-merits (FOMs) can be selected, contributing to overall cost reduction and performance improvement.

B. Performance Comparison

The state-of-art designs with similar topology structure and application are compared to the proposed work. Table II presents the comparison between the proposed DCX and existing counterparts based on switch electrical rating, transformer design, cost, peak efficiency, and prototype size. Multiphase half-bridge converter with current doubler rectifiers (MHB-CDH) [29] utilizes a magnetic structure that integrates the transformers and four-phase coupled inductors, and the transformer design is customized and complicated. Moreover, the switch electrical rating is unbalanced due to the difference duty cycle of switches in the half-bridge structure. Conventional *LLC* with matrix transformer [11] is the most mature solution to implement high efficiency and power density. Vicor's VTM current multiplier employing a sine amplitude converter [30] has a similar structure as *LLC* and it is another candidate for 48V-12V DCX. Sigma structure [13] employs extra regulation stages connected to DCX stage in series on the input side and in parallel on the output side. Thus, the voltage rating of primary-side switches is reduced. However, additional stages increase the topological complexity and the components count, resulting in higher costs. The designed prototype primarily aims at feasibility verification, with abundant test interfaces

TABLE II
PERFORMANCE COMPARISON WITH REPORTED COUNTERPARTS

Parameter	[29]	[11]	Vicor [30]	[13]	This work
Topology	MHB-CDH	Full-bridge *LLC*	Sine Amplitude Converter	Sigma Converter	SCSRC
Input	48 V	48 V	48 V	40 V-60 V	48 V
Output	1.8 V/4×30 A	12 V/20 A	12 V/25 A	12 V/30 A	12 V/25 A
Switching Frequency	600 *k*Hz	1.6 MHz	1.95 MHz	1MHz	1 MHz
Switch Electrical Rating	Unbalanced	Normal	Normal	Low	Lowest
Transformer Design	Complex	Normal	Normal	Normal	Easy
Cost	Low	Normal	Normal	High	Low
Peak Efficiency	93.1%	97.0%	>96%	<97.0% (V_{in}=48V)	97.23%
Size [mm^3]	42.2 × 18.6 × 4.5	20 × 31 × 8	32.5 × 22 × 10.04	44.5 × 33.8 × 8.2	59.5 × 30.6 × 7.8

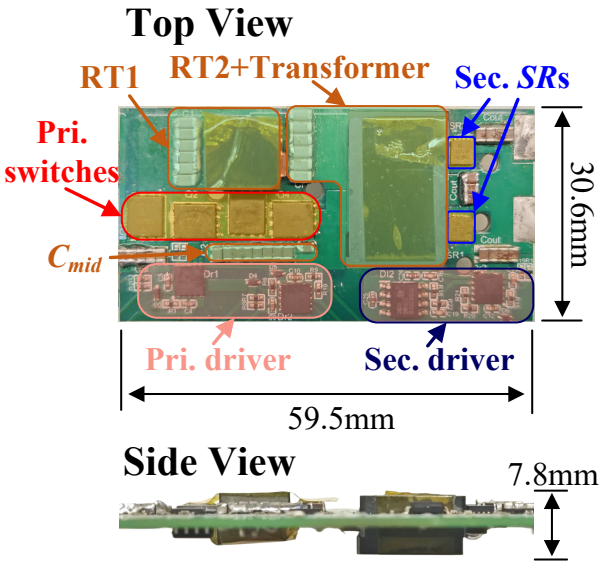


Fig. 12. Prototype of the proposed SCSRC converter.

such as current sensing ports integrated for convenient testing. Consequently, the pursuit of utmost power density has not been prioritized. Nevertheless, the proposed converter demonstrates competitive performance in terms of efficiency and power density due to simple transformer design and reduced switch stress.

TABLE III
SPECIFICATIONS OF PROTOTYPE

Symbol	Paramter	Value
V_{in}	Input Voltage	48 V
V_o	Output Voltage	12 V
P_o	Rated Power	300 W
f_s	Switching Frequency	1 MHz
$Q_1 - Q_4$	Primary Switches	BSC0501NSI
$SR_1, SR2$	Secondary synchronous rectifiers	BSZ013NE2LS5I
n	Transformer Turns Ratio	1
N/A	Core Material	DMR51W
C_1	Resonant Capacitor	282 nF
L_1	Resonant Inductor	120 nH
C_{mid}	Non-resonant Capacitor	100 μF
C_r	Resonant Capacitor	1.98 μF
L_r	Resonant (Leakage) Inductor	12 nH

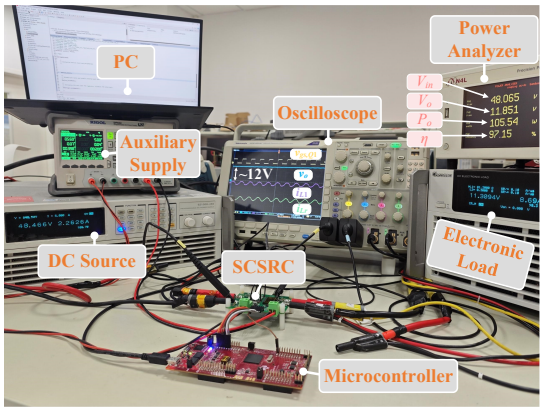


Fig. 13. Experimental setup and test bench.

VI. EXPERIMENTAL VERIFICATIONS

A hardware prototype of the proposed converter is constructed to validate the theoretical analysis and design considerations. The prototype is designed to operate at a frequency of 1 MHz, with an input voltage of 48V and 12V/25A output. The specifications of the prototype are outlined in Table III. Fig. 12 showcases the photo of the prototype, including top and side views. The effective volume, excluding debugging and I/O interfaces, measures 59.5 × 30.6 × 7.8 mm^3. Fig. 13 shows the experimental setup and test bench.

The experimental results are captured in Fig. 14. Fig. 14(a) and Fig. 14(b) capture the waveforms of the drain-to-source voltage v_{ds}, the gate-to-source voltage v_{gs}, and the resonant currents i_{L1} and i_{Lr} for Q_1 and Q_3 at full load, respectively. It is evident from the waveforms that ZVS operation is successfully achieved for both switches. Based on the symmetrical operations, it can be inferred that ZVS operation is also attained for Q_2 and Q_4.

Fig. 14(c) illustrates the resonant voltage and current waveforms in two resonant tanks. The waveforms of the middle bus voltage v_{mid}, the output voltage v_o, and the resonant current i_{L1} and i_{Lr} are presented in Fig. 14(d). Efficiency measurements are conducted using the N4L PPA4500 power analyzer, and the efficiency curve versus the output current is recorded in Fig. 15(a). The prototype achieves 97.23% peak efficiency at 6.5A output.

The loss breakdown of the prototype at full load is depicted in Fig. 15(b). Transformer loss includes both core loss P_{core} and copper loss P_{copper}, and inductor loss of L_1 is denoted as $P_{inductor}$ which can be calculated using FEA simulation. Semiconductor loss consists of both switching loss

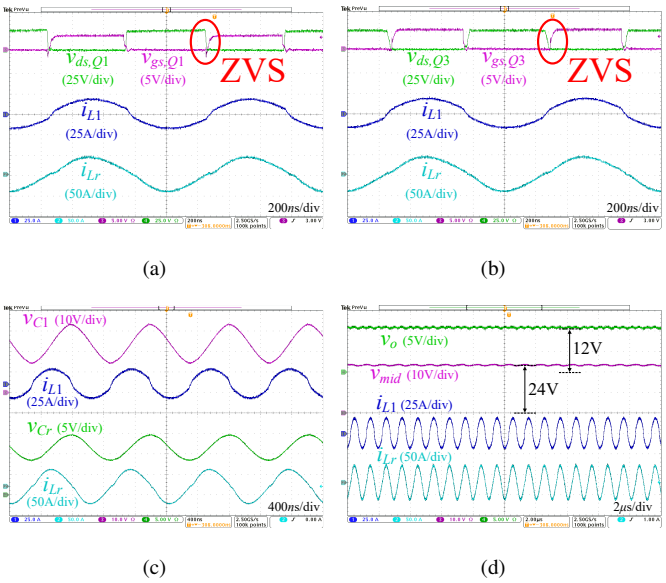


Fig. 14. Experimental results: (a-b) the drain-to-source and gate-to-source voltage waveforms of$Q_{1,3}$, and the resonant current waveforms of L_1 and L_r. (c) the resonant voltage and current waveforms in two resonant tanks. (d) the voltage waveforms of C_{mid}, C_o, and the resonant current waveforms of L_1 and L_r.

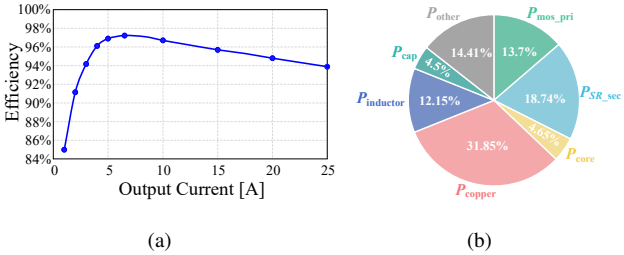


Fig. 15. (a) Measured efficiency versus output current. (b) Loss breakdown at full load (300W).

and conduction loss. Due to the ZVS turn-ON for all primary-side MOSFETs and ZCS turn-OFF for secondary-side SRs, the power loss P_{mos_pri} of primary-side MOSFETs primarily attributes to the MOSFET turn-OFF loss and the conduction loss, while the power loss P_{SR_sec} of secondary-side SRs is mainly the conduction loss. Furthermore, capacitor loss P_{cap} can be evaluated using their equivalent resistances and RMS currents. Other losses P_{other} are caused by parasitic resistances in the circuit loop and terminal connection losses. For ease of testing, the additional test interfaces results extra footprint and consequent losses. Additionally, the copper thickness is only 1oz due to cost considerations, and parallelization through multi-layer boards may lead to contact losses at terminal connections. The standardized manufacturing processes can minimize the portion of losses.

VII. Conclusion

In this paper, we propose a hybrid DCX based on switched-capacitor series-resonant converter in data center applications. The converter achieves $4n$:1 conversion ratio using an n:1 transformer, simplifying the transformer design. Notably, the proposed topology significantly reduces the voltage and current stress on primary switches compared with the conventional HB *LLC* with identical turns ratio. The resonant current of the SC cell enables ZVS for all primary switches. The magnetizing current does not contribute to the ZVS of primary switches and can be minimized. This advantageous feature allows the converter to operate at the optimal frequency, resulting in enhanced performance.

A 300W hardware prototype that converts 48 V input to a 12 V/25 A output is designed and tested. The experimental results validate the analysis and demonstrate the feasibility of the proposed converter design. This work highlights the potential of the proposed converter in meeting the demanding requirements of 48V bus power systems in data center applications.

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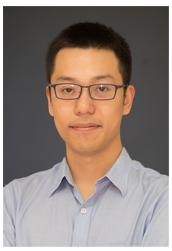

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