Overview of Voltage Regulator Modules in 48 V Bus-Based Data Center Power Systems

Jiawei LIANG, Liang WANG, Minfan FU, Junrui LIANG, and Haoyu WANG

***Abstract*—The intermediate dc bus voltage in modern data center backend power supply is evolving from conventional 12 V to 48 V. It still requires the voltage regulator modules (VRM) to feed the terminal loads such as memory and computing units operating with very high current (> 100 A/module) and very low logic voltage (0.8 V–1.8 V). This makes it challenging to optimize the design of load-side VRMs with quadrupled input voltage. This paper comprehensively reviews the state-of-the-art 48 V VRMs and categorizes them according to passive component utilization. The first category is inductive solution which is further divided into coupled-inductor-based converters and transformer-based converters. The second category named capacitive solution is further divided into resonant switched-capacitor-based converters (Resonant SCC) and hybrid switched-capacitor-based converters (Hybrid SCC). Typical topologies are discussed, analyzed and summarized to perform a comprehensive performance comparison, such that the characteristics of different VRMs can be manifested. Some design considerations are also given to facilitate the design of the practical prototypes. Moreover, opportunities and challenges in the future data center power system are presented to provide technical insights.**

***Index Terms*—Data center, 48 V, high efficiency, high power density, voltage regulator modules.**

I. Introduction

In recent years, with the rapid development of emerging information technologies such as 5G communication, big data, artificial intelligence, blockchain, and cloud computing, centralized computation, and storage in data center are booming. To meet these growing requirements, a large number of large-scale data centers for data computing, processing, and storage are built, and data center is becoming the critical infrastructure to support proper functioning of modern societies.

Data centers are enabled by electric power. Thus, energy consumption with the rapid rise of data centers is growing dramatically as well. As the major energy consumer, modern data center consumes nearly 3% world's electricity production, and it is predicted that the energy consumption of global data centers will reach 8% of total worldwide electric power consumption by 2030 [1]. However, less than half of the total energy is delivered to the terminal load, such as CPU, GPU, memory, and disk, while the rest is lost during power conversion, distribution, and cooling. This results in high costs, large cooling equipment, and inefficient power utilization.

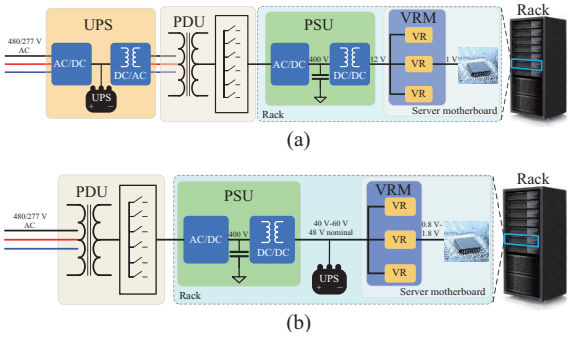

Fig. 1. Data center power architectures: (a) Conventional 12 V bus power architecture; (b) Emerging 48 V bus power architecture.

According to the statistics in [2], servers and cooling systems are the major energy consumer in data center. The utility cost exceeds the IT devices cost, and becomes the major cost in data center. Moreover, energy consumption and cooling impact the environment and contribute to global carbon emission [3]. Optimizing power solutions can relieve the burden of cooling systems, improve energy efficiency, and reduce carbon emissions. Therefore, it is deemed as the driving force of greener data centers.

The traditional power system in data center utilizes a 12 V bus with voltage regulator modules (VRMs) to power the terminal loads [4], as shown in Fig. 1(a). In 2020, the power consumption of 84% server rack has exceeded 10 kW [3], and it is estimated that the average power of a single rack in global data centers would reach 25 kW in 2025. With the fast increase of the power rating of server rack, high bus-bar copper loss, complexity, and utility cost gradually become the bottlenecks of 12 V bus system. These issues prompt the proposal of more efficient power systems. Fig. 1(b) illustrates the new generation 48 V bus power system [5], [6], where the rack bus voltage is stepped up from 12 V to 48 V and the bulky online uninterruptible power supply (UPS) is replaced by a local compact dc 48 V UPS. Consequently, lower bus-bar copper

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All authors are with the Center for Intelligent Power and Energy Systems, School of Information Science and Technology, ShanghaiTech University, Shanghai 201210, China. (e-mail: liangjw@shanghaitech.edu.cn; wangliang1@shanghaitech.edu.cn; fumf@shanghaitech.edu.cn; liangjr@shanghaitech.edu.cn; wanghy@shanghaitech.edu.cn).

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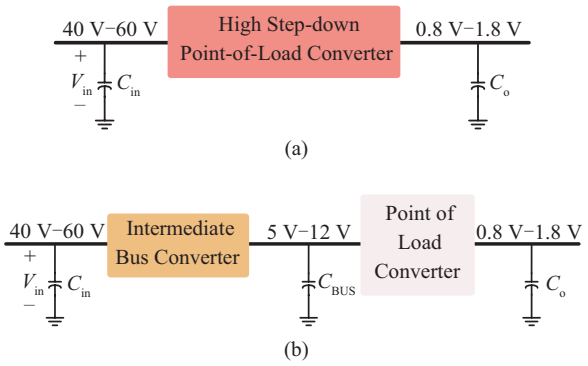

Fig. 2. Mainstream VRM structures: (a) Single-stage; (b) Two-stage.

loss ($P = I^2R$) and fewer power conversion stages are beneficial to improve the overall efficiency. Nevertheless, the quadrupled input voltage requires 48 V bus power system with a larger step-down ratio VRMs, which poses significant challenges to the VRM, which feeds power to the CPU/GPU loads with very high current (> 100 A/module) and very low logic voltage (0.8 V–1.8 V). Furthermore, high conversion efficiency, high power density, and low cost are the major desired features for the 48 V VRM located in the vicinity of terminal loads.

In this paper, the structure of VRMs in 48 V bus-based data center will be firstly introduced in Section II. Then, Section III categorizes the 48 V VRM solutions based on the passive components. Subsequently, the structure characteristics, advantages, and disadvantages of various VRM solutions are discussed and detailed in Section IV and Section V. A comprehensive comparative analysis is carried out in Section VI. Moreover, some practical issues are considered in Section VII. Finally, Section VIII presents the opportunities and challenges in the future data center power system, and Section IX concludes this paper.

II. VRM Structures for 48 V Power Architecture

As shown in Fig. 2, the mainstream 48 V VRMs have single-stage structure and two-stage structure, respectively. To clarify the category of VRM structure, the large intermediate bus decoupling capacitor serves as a typical criterion to distinguish the structure of 48 V VRMs. In other words, the two-stage structures with decoupling operation are defined as two-stage structures, while other non-decoupled multi-stage structures without large decoupling capacitors are still classified as single-stage structures. Single-stage structure utilizes a high step-down single-stage point-of-load (PoL) converter to directly convert the bus voltage (40 V–60 V, nominal 48 V) to the required load voltage (e.g. 0.8 V–1.8 V). Alternatively, in the two-stage structure, the front end stage employs a non-regulated intermediate bus converter (IBC) that converts 48 V to an intermediate voltage of 5 V–12 V, and then a PoL converter is utilized to regulate the intermediate voltage to 0.8 V–1.8 V that can be used by the terminal loads.

Although a single-stage structure has the potential to achieve higher energy efficiency and power density, the ultra-high step-down ratio almost reaches 50. This makes the practical application of existing single-stage structures limited due to the complex topology and control method. In contrast, the two-stage structure reutilizes the 12 V legacy power system and is more popular at present. Moreover, the two-stage structure also has good deployment flexibility and transient performance [7]. However, a large decoupling capacitor exists between the two stages to achieve power decoupling. This limits the power density and efficiency of the two-stage structure. Nevertheless, both single-stage structures and two-stage structures are valuable in terms of research. Designing VRM with high conversion efficiency, high power density (i.e. compact and thin), and low cost are the main evaluation directions.

III. Categories of 48 V VRM Solutions

With the gradually recognized superiorities of 48 V bus power system, many valuable solutions have been proposed to improve the performance of the 48 V VRMs. As the primary player for energy storage and transfer, passive components can be used as key for 48 V VRMs classification. As shown in Fig. 3, the first category is named as an inductive solution, which can be further divided into coupled-inductor-based converters and transformer-based converters. The second category is named capacitive-based solution, which can also be further divided into resonant switched-capacitor-based converters (Resonant SCC) and hybrid switched-capacitor-based converters (Hybrid SCC).

For the inductive solution, conventional pulse-width-modulation (PWM) converters, such as Buck, are constrained by the limited duty cycle. They exhibit poor performance with a high step-down conversion ratio. To address this issue, various coupled-inductor-based converters, which can provide a wide conversion ratio with a proper duty cycle, are proposed. On the other hand, transformer-based converters can also achieve high conversion ratio with satisfactory efficiency. Therefore, they are both good candidates for 48 V bus data center power systems.

As an alternative, capacitive-based solution is also popular in 48 V VRMs. Since capacitors possess higher energy density than inductors [8], switched-capacitor-based converters (SCC) eliminate magnetic components and only employ the capacitors to transfer energy. Thus, they have the potential to enhance the power density effectively. However, harsh transient currents might occur when the capacitors are reconfigured, which leads to severe charge redistribution loss. Correspondingly, inductors can better shape the transient currents. To improve, resonant SCC can achieve soft charging by inserting small inductors into SCC. This helps to eliminate the charge redistribution loss of capacitors without seriously sacrificing power density. Besides, in a single-stage structure with two-stage converters, hybrid SCC converter combines the operation of first-stage SCC and second-stage PoL converter to eliminate the bulky intermediate bus capacitor. It can also handle the harsh transients during capacitor reconfiguration. Moreover, the hybrid structure has two additional advantages: 1) the inductor current of PoL is shared with SCC to achieve soft charging, and 2) the large

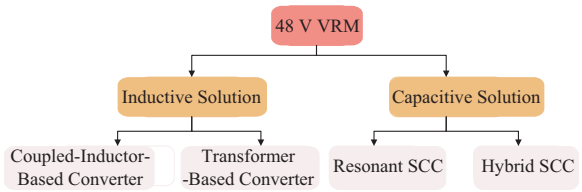

Fig. 3. Categories of 48 V VRM solutions.

intermediate decoupling capacitor between SCC and PoL is removed. Hence, the overall power density can be improved.

In Section IV and Section V, the evolution of each category of 48 V VRMs with respective major topologies and the performance are described in detail.

IV. Inductive Solutions

Inductive solutions utilize magnetic components to store and transfer energy. As shown in Fig. 3, inductive solutions include coupled-inductor-based converters and transformer-based converters.

A. Coupled-Inductor-Based Converters

Buck converter is the most classical and popular topology to step-down voltage due to its simple structure and control. Multiphase synchronous rectifier (SR) buck converter is still widely used as the PoL converter in data center applications. In the conventional Buck converter, the voltage gain equals the duty cycle of the active transistor. Thus, the duty cycle is ultra-low with a high voltage conversion ratio. This extremely low duty cycle leads to challenges of extremely short on state, demanding device switching speed, ultra-high current stress, as well as poor device utilization. To achieve a high step-down ratio with a proper duty cycle, a coupled-inductor is introduced to the Buck circuit. Fig. 4(b) shows a tapped-inductor buck converter [9]–[12] which can achieve a high step-down ratio by adjusting the duty cycle or the turn ratio of the coupled inductors. However, the leakage inductance of the tapped inductor produces a high voltage spike during switching transitions. This causes high switching losses and high voltage stress to accelerate device damage, and results in increased cost and reduced efficiency. Furthermore, large magnetizing inductor current corresponds to a large tapped-inductor core, which limits the power density. To suppress the voltage spike caused by the leakage inductance, a tapped inductor buck converter with a series capacitor is proposed in [13]. As shown in Fig. 4(c), the additional series capacitor C_B resonates with the leakage inductor. This helps suppress the voltage spike and achieve soft switching. Meanwhile, C_B can withstand part of the voltage and improve the step-down ratio. To further improve the step-down ratio, the topology of Fig. 4(d) is proposed in [14], a higher step-down ratio can be achieved due to the multiple capacitor units. Although its dc magnetizing current is reduced, the required magnetic core is still bulky. In [15], a high step-down converter with zero dc magnetizing current and non-pulsating output current is presented, as shown

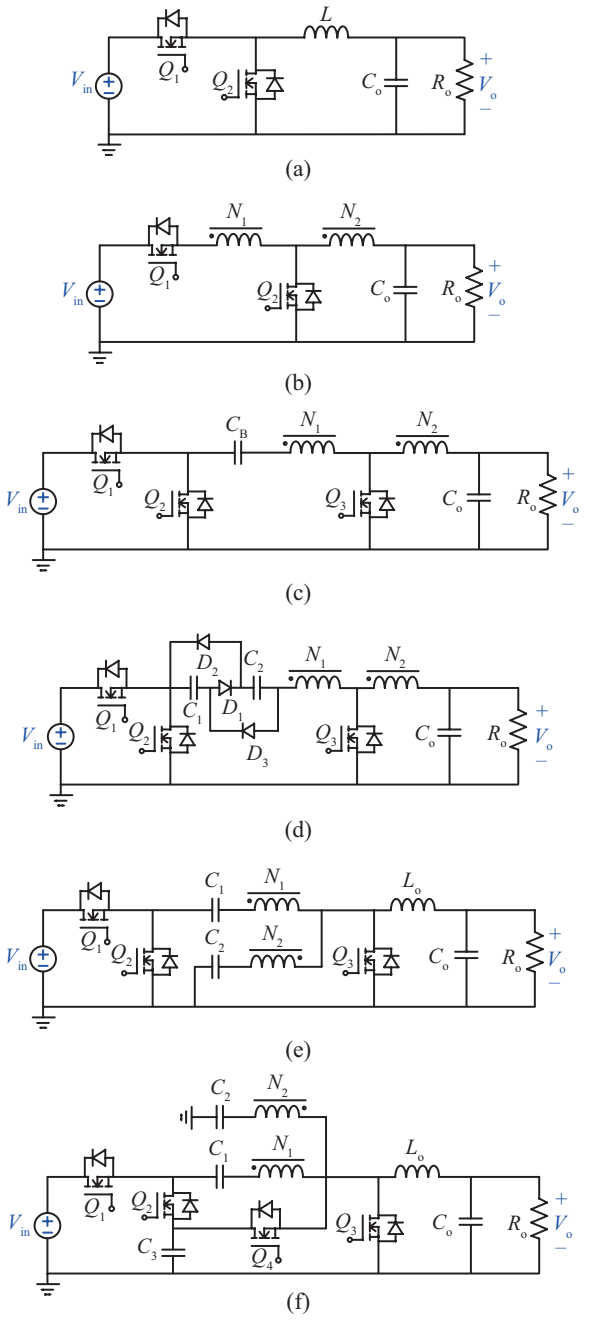

Fig. 4. Coupled-inductor-based converters: (a) Conventional buck; (b) Tapped-inductor buck [9]–[12]; (c) Ultrahigh step-down converter [13]; (d) Step-down converter with wide voltage conversion ratio [14]; (e) High step-down converter with zero dc magnetizing current and nonpulsating output current [15]; (e) Modified high step-down converter [16].

in Fig. 4(e). Owing to the zero dc magnetizing current, the magnetic core size of the coupled inductor can be significantly reduced with lower core loss. Fig. 4(f) illustrates a modified high step-down converter [16] which is derived by adding an auxiliary circuit consisting of an extra small capacitor C_3 and a MOSFET Q_4 to the topology of Fig. 4(e). Correspondingly, the flux linkage of the coupled inductor is reduced. In addition, the voltage spike of Q_4 can be reduced due to the auxiliary circuit, and the converter exhibits a higher step-down ratio. Table I

TABLE I
DC MAGNETIZING CURRENT, VOLTAGE GAIN AND IDEAL VOLTAGE STRESS FOR ABOVE COUPLED-INDUCTOR-BASED CONVERTERS

Topology	Voltage Gain	dc Magnetizing Current	Ideal Voltage Stress
Tapped-inductor buck [9]–[12]	$D\frac{N_2}{N_1(1-D)+N_2}$	$I_o(\frac{N_2}{N_1}+\frac{DN_2}{N_1(1-D)+N_2})$	$V_{ds1}=\frac{N_1+N_2}{N_1(1-D)+N_2}V_{in}$ $V_{ds2}=\frac{N_2}{N_1(1-D)+N_2}V_{in}$
Ultrahigh step-down converter [13]	$D\frac{N_2}{N_1+N_2}$	$I_o\frac{N_1}{N_2}$	$V_{ds1}=V_{ds2}=V_{in}$ $V_{ds3}=\frac{N_2}{N_1+N_2}V_{in}$
Step-down buck with widevoltage conversion ratio [14]	$D\frac{N_2}{N_1(1+D)+N_2}$	$I_o(\frac{N_2}{N_1}-\frac{DN_2}{N_1(1+D)+N_2})$	$V_{ds1}=V_{ds2}=V_{in}$ $V_{ds3}=\frac{N_2}{N_1(1+D)+N_2}V_{in}$
High step-down converter with zero dc magnetizing inductance current [15]	$D\frac{N_2}{N_1+N_2}$	0	$V_{ds1}=V_{ds2}=V_{in}$ $V_{ds3}=\frac{N_2}{N_1+N_2}V_{in}$
Modified high step-down converter [16]	$D\frac{N_2}{N_1+2N_2}$	0	$V_{ds1}=V_{ds2}=\frac{N_1}{N_1+N_2}V_{in}$ $V_{ds3}=V_{ds4}=\frac{N_2}{N_1+2N_2}V_{in}$

compares the dc magnetizing current, voltage gain, and ideal voltage stress for the above topologies.

Coupled-inductor-based converters are generally adopted in low-power applications (< 50 W) [13], such as DRAM and hard disk. This is due to their advantages of few components, simple structure and low cost. In high-power applications, transformer-based converters as another inductive-based 48 V VRM are widely investigated.

B. Transformer-Based Converters

A high-frequency transformer can achieve a high voltage conversion ratio and is widely used in high efficiency and high power density topologies. In [17], a load-dependent soft switching method in half-bridge current doubler converter is proposed to achieve zero-voltage-switching (ZVS) over the entire load range with increased light load efficiency. The PoL based on impedance-control-network (ICN) resonant converter architecture [18] can also achieve a large step-down, and meanwhile, maintain high efficiency over wide input voltage and power ranges. In [19], a self-driven ZVS full-bridge converter is proposed to reduce the gate driving loss and improve driving speed. Thus, the switching frequency can reach several MHz, which leads to higher power density. Although there are many transformer-based converters, the most popular transformer-based topologies are *LLC* resonant converters due to the ZVS for primary-side MOSFETs and zero-current-switching (ZCS) for secondary-side diodes. Fig. 5 shows the half-bridge structure and full-bridge structure of *LLC*.

However, bulky transformer limits the power density of *LLC*

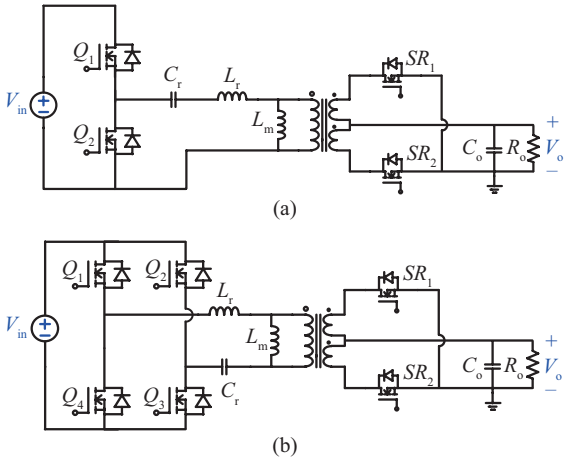

Fig. 5. *LLC* converter: (a) Half-bridge structure; (b) Full-bridge structure.

converter, while pulse frequency modulation increases control complexity and reduces conversion efficiency. Therefore, operating the *LLC* at its resonant frequency as a dc transformer (DCX) can achieve optimal efficiency, and the control is relatively simple.

A typical *LLC*-based two-stage 48 V VRM is proposed in [20]–[23], the full-bridge *LLC* DCX realizes the preliminary voltage step-down, and then the multi-phase buck converter is responsible for the back-end voltage regulation. In particular, the planar transformer is optimized to improve the power density and to reduce magnetic loss. Nevertheless, at light load, a large circulating current in the *LLC* transformer degrades the conversion efficiency. To handle this issue, phase shedding for

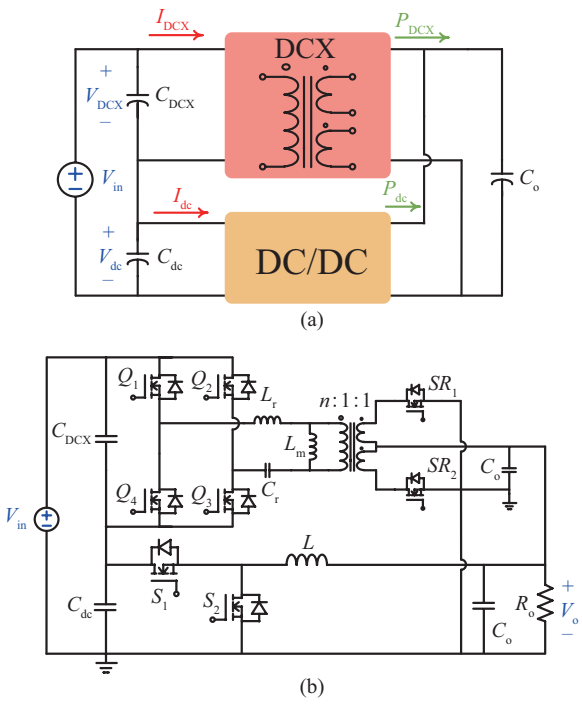

Fig. 6. (a) Sigma structure [24]–[26]; (b) Sigma converter: *LLC* DCX + Buck [22], [27], [28].

multiphase buck and dynamic reconfiguration between half-bridge *LLC* and full-bridge *LLC* at different loads are adopted [20] to reduce the losses and to improve light-load efficiency.

Generally, more energy conversion stages lead to lower overall system efficiency and power density. Therefore, single-stage solution is expected to outperform in conversion efficiency and power density. It becomes one of the focuses of data center research. A single-stage sigma structure is proposed in [24]–[26], as shown in Fig. 6(a), it links two converters with series input and parallel output. The unregulated DCX delivers the main power and the parallel small dc/dc converter regulates the output voltage. A potential benefit is that it can achieve higher conversion efficiency, and proper selection of DCX and dc/dc topology can maximize its advantages. The soft-switching characteristics of *LLC* converters enable operation at very high frequency (MHz), thereby reducing the size of the magnetic components, enabling both high efficiency and high power density. Therefore, *LLC* is a good candidate as the DCX to deliver power. Fig. 6(b) shows a sigma converter combining *LLC* DCX and buck [22], [27], [28]. As the input currents of the two converters are identical, the input voltage across each module determines the power distribution in between, and the overall system efficiency can be increased significantly due to the current sharing. The power relationship of two modules [27] can be expressed as,

$$\frac{P_{\mathrm{DCX}}}{P_{\mathrm{dc/dc}}}=\frac{V_{\mathrm{DCX}}}{V_{\mathrm{dc}}},\ I_{\mathrm{DCX}}=I_{\mathrm{dc}} \tag{1}$$

The structure and control method of *LLC* DCX are simple. The magnetic component design of *LLC* transformer becomes a research focus to further optimize the performance of the transformer-based converter. Detailed magnetic design is discussed in Section VII.

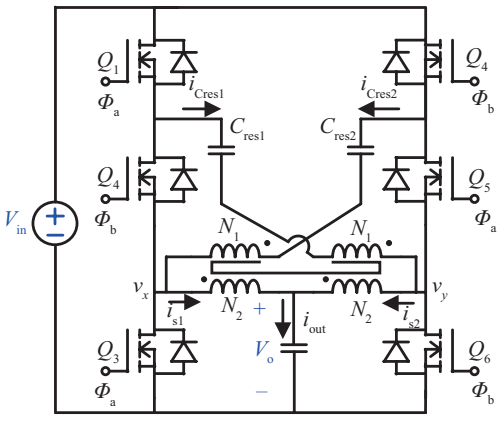

Fig. 7. Hybrid converter with a multi-tapped autotransformer [29].

In addition to *LLC* DCX, Infineon Technologies has recently focused on a non-isolated transformer-based DCX converter consisting of an interleaved SCC and a multi-tapped autotransformer (MTA) [29]. Compared with an *LLC*, it has lower current stress both at MOSFETs and magnetic components, and higher efficiency due to its outperforming robustness against components mismatch. As an alternative to *LLC* DCX, it can also be used in Sigma structure [30], and has a lower turns ratio with a step-down ratio identical to *LLC*. This mainly attributes to its SCC structure. The topology is illustrated in Fig. 7.

V. Capacitive Solutions

In high power density applications, magnetic-less topologies are desired due to the elimination of magnetic components. The higher energy density of capacitors makes switched-capacitor-based converters and their derivative topologies attractive. In data center applications, SCC converters are generally used as a front-end non-regulated stage with a fixed step-down ratio in a two-stage structure. Fig. 8 shows four classic SCCs. They are Ladder structure, Dickson structure [31], series-parallel [32], and Fibonacci [33]. A numerical comparison of the number and voltage rating of components for those SCCs is summarized in Table II.

In SCC, only capacitors are employed to transfer energy, and the magnetic components are eliminated. Hence, the power density can be effectively enhanced. However, harsh transient currents might occur when the capacitors are reconfigured, which leads to severe charge redistribution loss. If an inductor is connected to the capacitors during the switching, then soft charging of the capacitors is achieved and energy loss is eliminated. Resonant SCC and hybrid SCC are two solutions to achieve soft charging.

A. Resonant Switched-Capacitor-Based Converters

Resonant SCC is derived by inserting small inductors into SCC to form resonant tanks so that the transient currents can be suppressed. Fig. 9 illustrates two types of inserting small

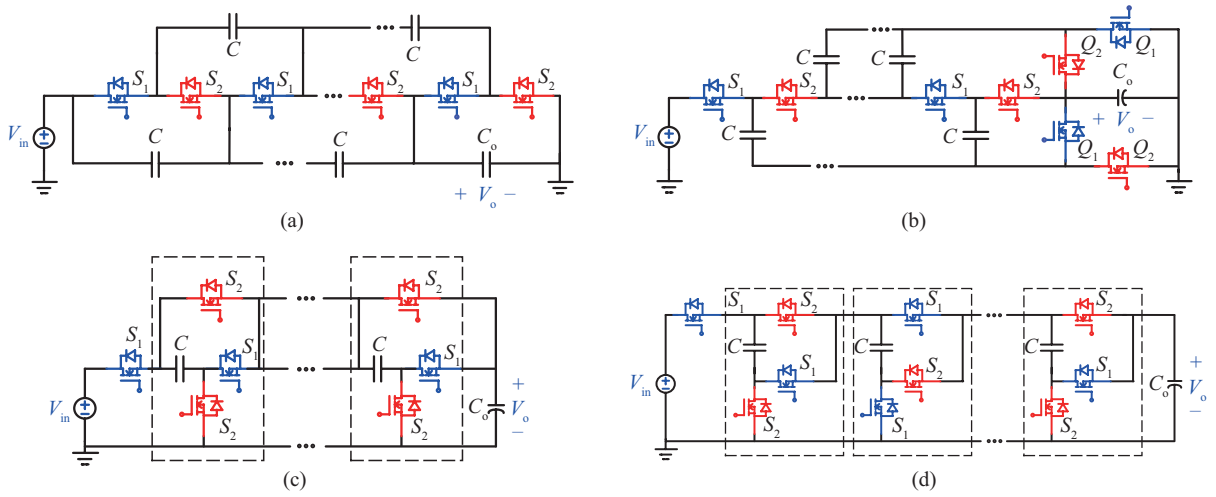

Fig. 8. Switched-capacitor converters: (a) Ladder structure [31]; (b) Dickson structure [31]; (c) Series-parallel structure [32]; (d) Fibonacci structure [33].

TABLE II
COMPARISON OF THE NUMBER AND VOLTAGE RATING OF COMPONENTS FOR SCCS

Topology	Voltage Gain	Switch Count	Voltage Stress of Switches	Flying Capacitor Count	Voltage Stress of Flying Capacitors
Ladder [31]	6:1	12	V_o (12 MOSFETs)	9	V_o (9 MOSFETs)
Dickson [31]	6:1	10	$2V_o$ (4 MOSFETs) V_o (6 MOSFETs)	5	$5V_o$ (1 MOSFETs) $4V_o$ (1 MOSFETs) $3V_o$ (1 MOSFETs) $2V_o$ (1 MOSFETs) V_o (1 MOSFETs)
Series-parallel [32]	6:1	16	$5V_o$ (3 MOSFETs) $4V_o$ (2 MOSFETs) $3V_o$ (2 MOSFETs) $2V_o$ (2 MOSFETs) V_o (7 MOSFETs)	5	V_o (5 MOSFETs)
Fibonacci [33]	5:1	10	$3V_o$ (2 MOSFETs) $2V_o$ (4 MOSFETs) V_o (4 MOSFETs)	3	$3V_o$ (1 MOSFETs) $2V_o$ (1 MOSFETs) V_o (1 MOSFETs)

resonant inductors into the 4:1 Dickson SCC converters, which are aggregated inductor type [34] and distributed inductor type [35]. Generally, the inductance of the distributed inductor is smaller, and it can utilize the stray inductor of printed-circuit-board (PCB). Hence, it is better than the aggregated inductor in power density. By optimizing the circuit loop of resonant SCC with distributed inductor in Fig. 9(b), the inductor L_2 can be removed, and the optimized topology called switched-tank converter (STC) [7], [36]–[38] is shown in Fig.10, the detailed derivation is discussed in [37]. In STC, small inductors resonate with the corresponding capacitors, which facilitates a soft charging of capacitors. ZCS of all MOSFETs is achieved, which effectively reduces the device switching loss and electromagnetic interference (EMI). However, multiple resonant tanks result in strict requirements of resonant parameters matching. The specific design considerations of resonant parameters and layout are discussed in Section VII.

Compared with ZCS-type resonant STC converter, the cascaded resonant converter proposed in [39] can operate in either ZCS or ZVS mode. As shown in Fig. 11(a), the proposed converter cascades two 2-to-1 SC converters to achieve a 4-to-1 step-down ratio, and each SC converter has an inductor in series in the output. This inductor is selected to resonate with the flying capacitor. When the switching frequency is matched to the resonant frequency, the converter can achieve ZCS operation. However, in practical implementations, it is difficult to guarantee ZCS operation due to the inevitable mismatch of resonant parameters. Fortunately, the two stages are decoupled by the intermediate capacitor C_{mid}. Hence, two resonant tanks are independent compared with the resonant tanks of STC. In this case, the cascaded converter can operate in ZVS mode without guaranteeing accurately matched resonance parameters as long as the switching frequency is slightly above the resonant frequency to compensate for parameter variations. In addition, ZVS mode, which can eliminate the switching loss caused by MOSFET C_{oss}, is better than ZCS mode at light-load. Although the decoupled operation of two stages reduces the control complexity, the bulky decoupling capacitor ($C_{mid} \gg C_1 \& C_2$) is non-negligible in power density. To reduce the size of the intermediate capacitor, the author proposes a two-phase interleaved cascaded resonant converter with synchronous control of two stages to balance the amount of charge delivered

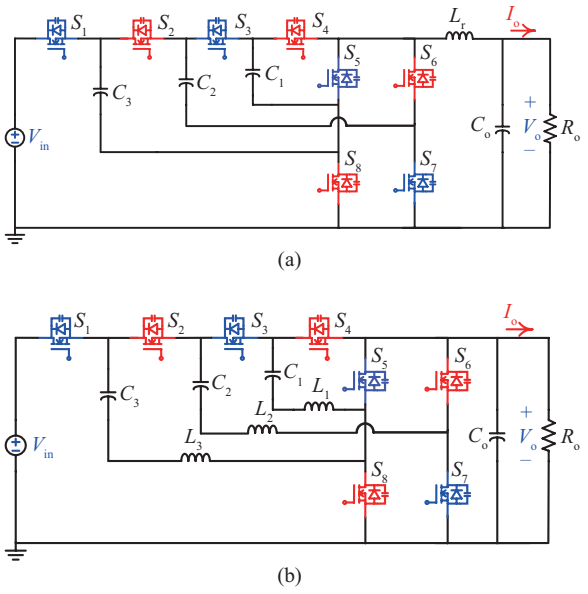

Fig. 9. 4-to-1 Dickson SCCs: (a) SCC with aggregated inductor [34]; (b) SCC with distributed inductor [35].

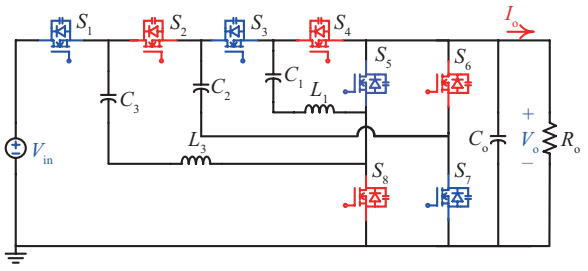

Fig. 10. Switched-tank converter [7], [36]–[38].

and removed from the intermediate capacitor at the same time, as shown in Fig. 11(b). Therefore, the voltage of the intermediate capacitor is stable even without a large capacitor. Meanwhile, the interleaved structure supports higher current which mitigates the current stress of the second stage. Based on this interleaved structure, an optimized topology [40] which merges the first stage into one phase is proposed to improve power density. As shown in Fig. 11(c), the current of L_1 is matched with the current of L_{21} in half period while is matched with the current of L_{22} in the other half period. Therefore, almost zero current flows through C_{mid}. This leads to a low-profile intermediate capacitor.

For two-stage 48 V VRMs, optimizing the intermediate bus voltage is beneficial to further improve the overall efficiency. This is because the FETs in the multiphase buck converter have lower breakdown voltage. Thus, FETs with better figure-of-merits (FOMs) can be selected [23]. The above-mentioned resonant SCC exhibits a 4-to-1 voltage conversion ratio. It cannot be easily extended to lower bus voltage without obvious performance sacrifice. In [32], a multi-resonant-doubler converter as illustrated in Fig. 12 is proposed to achieve a higher step-down ratio by combining different capacitors. Compared with other 8:1 SCC topologies, it can achieve an 8:1 step-down ratio with fewer components. As a compromise,

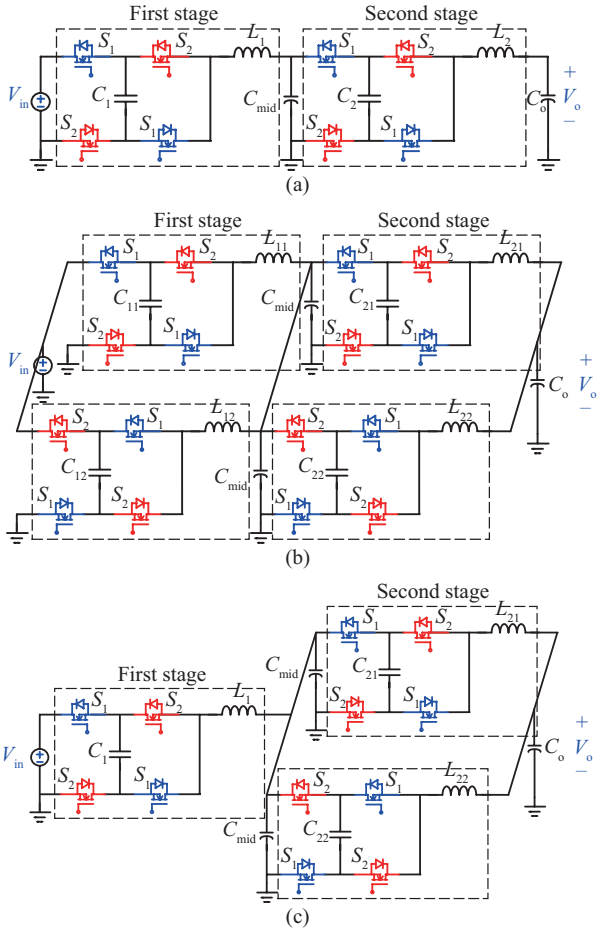

Fig. 11. 4-to-1 resonant SCCs: (a) Cascaded resonant converter [39]; (b) Two-phase cascaded resonant converter; (c) Two-phase cascaded resonant converter with first stage merged into one phase [40].

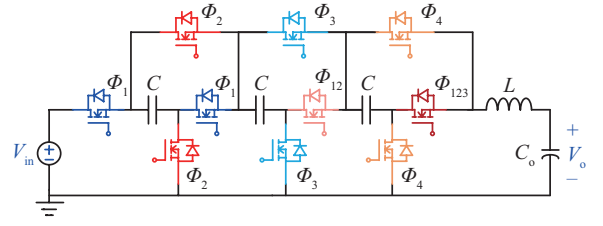

Fig. 12. 8-to-1 multi-resonant-doubler converter [32].

it requires multiple pairs of driving signals, and the flying capacitors suffer from higher voltage ratings.

Typically, the SCC converters with a fixed conversion ratio are driven by several pairs of complementary signals. In contrast, a regulated SCC converter named dual-active-bridge (DAB) derived hybrid SCC is proposed [41]. Fig. 13 shows the topology derived by inserting an inductor in Dickson SCC. Although hard switching still exists in certain switches, the good voltage regulation is scalable and can handle a wide range of variable switching frequency operations.

B. Hybrid Switched-Capacitor-Based Converters

The decoupled two-stage capacitive solution for 48 V VRM requires the inserting of the extra inductors into SCC stage to

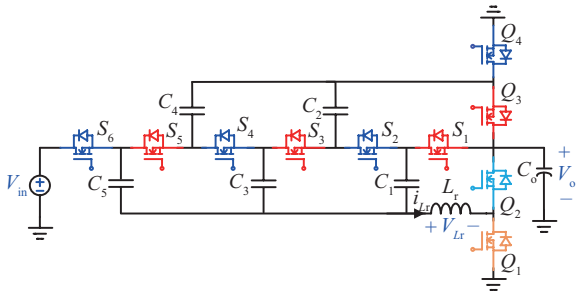

Fig. 13. Dual-active-bridge derived hybrid SCC [41].

achieve soft charging. Alternatively, a hybrid SCC converter can also eliminate the charge redistribution loss of the flying capacitor by utilizing the second-stage current. The hybrid two-stage converter removes resonant inductors and the large intermediate decoupling capacitor, and merges the operation of the front-end unregulated step-down converter and back-end regulated converter. For instance, the hybrid Dickson converter [42] can be considered the most basic hybrid SCC which merges a Dickson SCC and a Buck. Interestingly, the topology is similar to the one in Fig. 9(a), but the operating principles are different. Here the inductor is no longer used for resonance. It serves as the inductor of the buck stage to provide a stable current source to realize the soft charging of the flying capacitor in SC stage. In addition, the bridge side switches are multiplexed by the SC stage and buck stage with the unique split-phase driving sequence. The drawback of this converter is exposed to a high conversion ratio and high output current applications due to the single-phase and small duty cycle of Buck. Consequently, a dual-inductor-hybrid (DIH) converter is proposed [43], as shown in Fig. 14(a). It employs two interleaved inductors at the output and eliminates two large synchronous switches on the bridge side. As the result, the conduction loss is reduced due to fewer components in the loop. A higher current rating is feasible by exploiting the interleaved inductors. Furthermore, a symmetric DIH converter shown in Fig. 14(b) can further improve the component utilization and naturally balance the currents of two interleaved inductors and all switches, which simplifies component selection, improves electrical and thermal performance and reduces cost [44]. However, the ultrahigh current rating is still an undesired issue for these converters.

The recently proposed linear-extendable-group-operated PoL (LEGO-PoL) architecture [45]−[48] is well suited for high step down ratio and ultrahigh output current applications. One sub-module of the LEGO-PoL architecture including a 2-to-1 SC unit and a multiphase buck unit is illustrated in Fig. 15(a). Fig. 15(b) shows the N sub-modules of the LEGO-PoL architecture. As shown, many 2-to-1 SC units are connected in series to split the input voltage, and many multiphase buck units are paralleled to split the output current. The merged two-stage structure eliminates the decoupling capacitor, and then the inductor current of the multiphase buck is used as current source to achieve soft charging and soft switching of the SC units. While the SC units are utilized to ensure current sharing among the multi-phase buck. Therefore, it is featured with

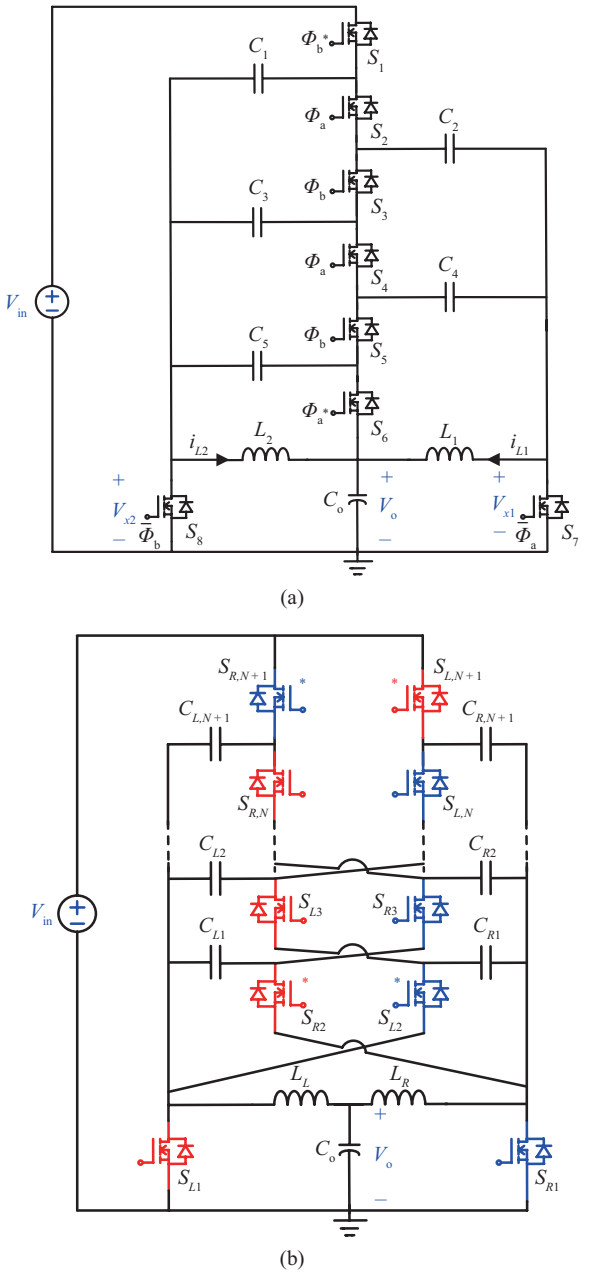

Fig. 14. Hybrid Dickson SCCs: (a) Dual-inductor-hybrid (DIH) converter [43]; (b) Symmetric DIH converter [44].

automatic voltage balancing and current sharing. This helps to reduce its control complexity. On the other hand, the coupled inductors employed in multi-phase buck can significantly boost the power density of LEGO-PoL. The comparison of the commercial discrete inductors and the customized coupled inductors used in a four-phase buck is illustrated in Fig. 16 and the specific parameters are listed in Table III [46]. The results show that the volume of the coupled inductors is only 57.7% of that of four discrete inductors, and the dc resistance is only 25%, the leakage inductance and core losses are also lower. In addition, the energy storage requirements of the magnetic core of coupled inductors are lower. This leads to a more compact core size and a faster transient response.

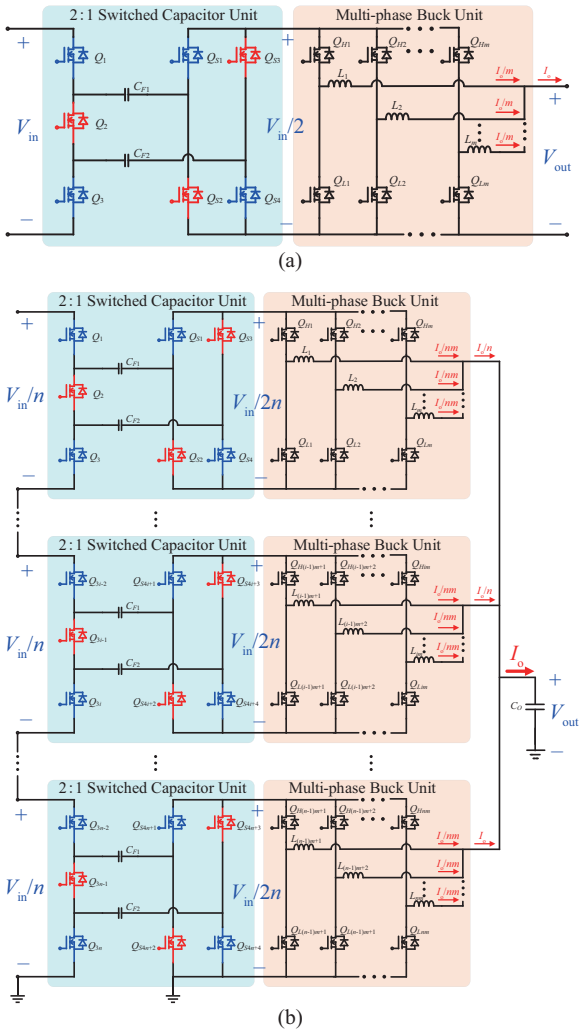

Fig. 15. Linear-extendable-group-operated PoL (LEGO-PoL) architecture [45]–[48]: (a) One sub-module; (b) N sub-modules.

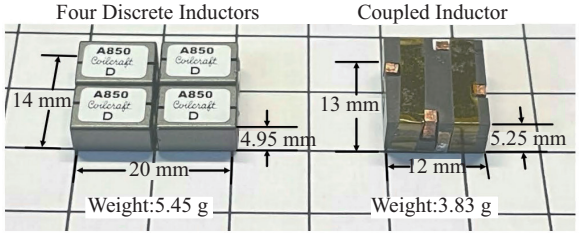

Fig. 16. Comparison of the coupled inductors with four discrete Coilcraft SLR1050A 85 nH discrete inductors [46].

Another hybrid SCC for direct 48 V-to-PoL conversions with ultrahigh current is Dickson^2-PoL converter [49]. The schematic of the proposed Dickson^2-PoL converter is shown in Fig. 17. As shown, it is also highly modular, easy to control, and naturally balanced. This converter consists of a 3-to-1 Dickson SC topology in the first stage and three identical synchronous controlled modules in the second stage. It should be noted that the synchronously controlled module merges a 3-to-1 Dickson SC with Buck topology. The intermediate capacitor is eliminated. Moreover, the double 3-to-1 Dickson

TABLE III
COMPARISON BETWEEN DISCRETE AND COUPLED INDUCTORS [46]

Symbol	Meaning	Discrete	Coupled
V_{in}	Buck Stage Input Voltage	8 V	
V_{out}	Output Voltage	1 V	
f_{buck}	Switching Frequency	1 MHz	
L_l	Phase Leakage Inductance	85 nH	12.4 nH
L_{tr}	System Transient Inductance	7.08 nH	1.03 nH
R_{dc}	Phase dc Resistance	0.39 mΩ	0.09 mΩ
P_c	System Core Loss	1.6 W	0.45 W
I_{sat}	Saturation Current	86 A	N/A
Δi_p	Phase Current Ripple	10.3 A	10.9 A
V	Total Volume	4.24 cm^3	2.45 cm^3

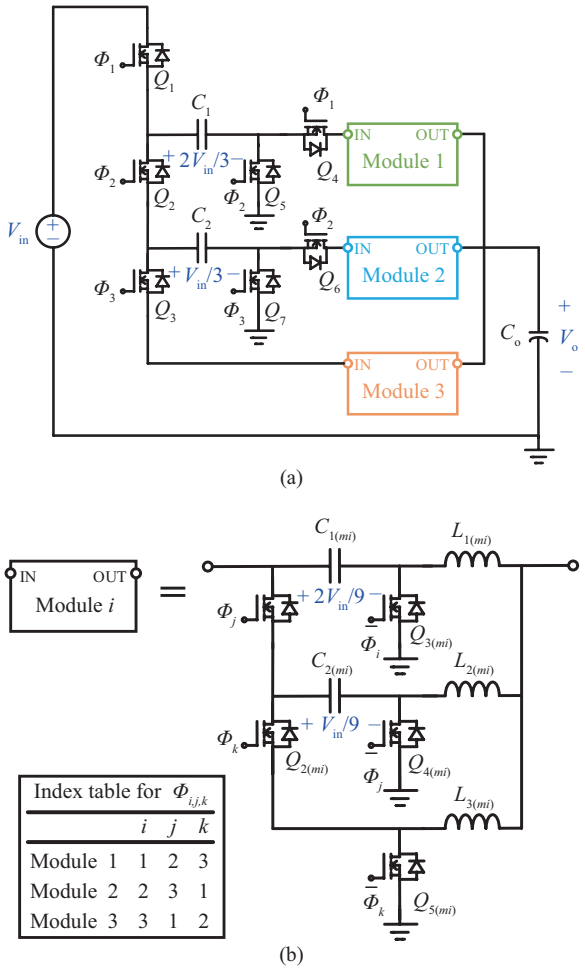

Fig. 17. Schematic of the Dickson^2-PoL converter [49]: (a) Overall architecture; (b) Modular structure i in Stage 2. The components labeled with the subscript (mi) are in Module i. The values of the label indexes (i, j and k) for circuit components and control signals (Φ_i, Φ_j and Φ_k) in each module are listed in the index table.

SC with a 9-to-1 step-down ratio reduces the conversion burden of the regulated buck converter.

VI. COMPARISON OF 48 V VRMS

Table IV compares the state-of-the-art for the 48 V VRMs in terms of voltage conversion ratio, power rating, soft-switching

TABLE IV
PERFORMANCE COMPARISON OF 48 V VRMS IN DATA CENTER POWER SYSTEMS

Structure		Topology	Category[1]	Input-Output	Soft Switching	Switching Frequency	Component Count[2]	Power Density (W/in^3)	Efficiency	
									@Peak	@Full Load
Two Stage	First Stage	STC [7]	3	60 V−10 V 600 W	ZCS	253 kHz	16/5/3/0	1000	98.55%	97%
		Cascaded Resonant SCC [39]		48 V−12 V 720 W	ZVS	100 kHz	8/3/2/0	2500 (only power stage)	99%	97.23%
		Two-phase Cascaded Resonant SCC with merged first stage [40]					12/4/3/0	4068 (only power stage)	99%	97.92%
		MRDC [32]		48 V−6 V 240 W		70 kHz	10/3/1/0	1675	98%	95.9%
		Hybrid converter [29]	2	48 V−6 V 750 W		500 kHz	6/2/0/2	8th brick size	98.15%	97%
		DAB derived hybrid SCC [41]	3	48 V−8 V−1.2 V 66 W		SCC: 350 kHz Buck: 700kHz	10/5/1/0 +6/0/3/0	470	91.9%	88.7%
		LLC DCX +buck [20]	2	48 V−12 V−1.8 V 240 W		*LLC*: 1.6 MHz Buck: 1 MHz	8/1/1/1 +8/0/4/0	*LLC*: 860	91%	87%
		Vicor: PRM+VTM [50], [51]	-	48 V−1 V 200 W		PRM: 1 MHz VTM: 1.4 MHz	-	153	90.1%	-
		ADI [52]		48 V−1 V 50 W	-	350 kHz		89	90.8%	88.1%
Single Stage		Ultrahigh step-down converter [13]	1	48 V−3.3 V 49.5 W	ZVS	100 kHz	3/2/1/0	170	95.1%	-
		Step-down buck with wide voltage [14]		48 V−1.2 V 30 W			6/3/1/0	-	90.2%	
		High step-down converter [15]		48 V−3.3 V 33 W			3/2/2/0		98.1%	
		Modified high step-down converter [16]					4/3/2/0	228	94.8%	
		Sigma: *LLC*+buck [28]	2	48 V−1 V 80 W	ZVS	*LLC*: 1 MHz Buck: 600 kHz	12/1/1/4 +2/0/1/0	420	93.5%	92.6%
		Hybrid SC Sigma [30]		48~51 V−5.1 V 750 W		450 kHz	9/4/1/2	1060	97.5%	95%
		LEGO -PoL [47]	4	48 V−1 V 780 W	ZCS	1 MHz	40/5/12/0	510	88.4%	78.7%
		Dickson^2-PoL [49]		48 V− 1.5 V/270 A 1.2 V/270 A 1 V/270 A	ZVS	289 kHz	22/8/9/0	137@1.5 V 111@1.2 V 91@1 V	93.5%@1.5 V 92.5@1.2 V 91.6@1 V	89.8%@1.5 V 88.9%@1.2 V 87.7%@1 V
		DIH [53]		48 V−3 V/50 A 2 V/60 A 1 V/70 A		750 kHz	8/5/2/0	524@3 V 419@2 V 246@1 V	93.8%@3 V 92.2%@2 V 87.5@1 V	91.1%@3 V 88.1%@2 V 80%@1 V
		SDIH [44]		48 V−3 V/45 A 2 V/66 A 1 V/105 A			10/6/2/0	768@3 V 751@2 V 598@1 V	89.8%@3 V 88.2%@2 V 83.5%@1 V	88%@3 V 83.4%@2 V 71.5%@1 V
		TI [54]	2	48 V−1 V 50 W	-	600 kHz	-	129	90.7%	87.7%

[1] 1: Coupled-inductor converter; 2: Transformer-based converter; 3: Resonant SCC; 4: Hybrid SCC;
[2] The number of switch/capacitor/inductor/transformer.

TABLE V
ADVANTAGES AND DISADVANTAGES OF 48 V VRMS IN DATA CENTER POWER SYSTEMS

Topology		Advantages	Disadvantages	Applications
Inductive Solution	Coupled-inductor-based converter	• High step-down ratio • Small number of components	• Low frequency • Large magnetics	• Low power • High step-down
	Transformer-based converter	• Isolation • Soft switching • High frequency	• Large magnetics • Complex magnetics design	• High voltage and high power rating • Isolations • High efficiency
Capacitive Solution	Resonant SCC	• High power density • Fast dynamic response • Soft charging and soft switching	• Sensitive to resonant parameters • Not easily extendable to lower voltage	• Two-stage structure as the intermediate bus converter • High efficiency and high power density • High power rating
	Hybrid SCC	• Soft charging • Single stage • Modularity	• Large number of components • Low light-load efficiency	• Ultrahigh power rating • High power density and high efficiency

performance, switching frequency, component count, power density, and peak and full load efficiency.

For the coupled-inductor-based converters, they can achieve a high step-down ratio by modulating the duty cycle and turns ratio with a low component count, but the lower operating frequency limits the power density due to larger magnetic components. They are usually used in low-power and high-step-down applications.

Transformer-based converters such as *LLC* are generally used in high-power applications with high efficiency due to their soft-switching characteristics. Although the transformer is bulky, the power density can be improved by integrated magnetics technologies of high-frequency transformer. In addition, it is suitable for isolated situations.

The resonant SCCs eliminate the bulky magnetic components and depends on the combination of switches and capacitors to achieve high step-down with a very high power density and fast dynamic response. By inserting a small inductor to resonant with capacitors, the current spike is suppressed when the capacitor voltages mismatch for soft charging and soft switching. However, the ZCS-type SCCs are very sensitive to resonant parameters if there are multiple resonant tanks. In addition, they generally operate with a fixed step-down ratio, and it is not easy to achieve a higher step-down ratio. Therefore, resonant SCCs are usually employed in a two-stage structure of 48 V VRM as the intermediate bus converters and are suitable for high efficiency and high power density applications.

Compared with resonant SCC in a two-stage solution, hybrid SCC merges the control of two stages and removes the large intermediate decoupling capacitor. The modular design can achieve higher power density and support ultrahigh output currents, but the light-load efficiency is limited due to a large number of components.

A detailed summary of 48 V VRM based on the aforementioned categories is depicted in Table V which includes the advantages, disadvantages, and suitable applications.

VII. DESIGN CONSIDERATIONS OF 48 V VRMS

In the practical implementations, some design considerations such as component selection, magnetic design, control scheme, and PCB layout play an important role in VRM performances, and different types of VRMs have different focuses on design. Therefore, this section introduces some necessary design considerations for data center 48 V VRMs. Subsequently, the transformer design of *LLC* and the resonant component selection of STC are selected as the case study. They also have good reference value for other topologies with similar structures or operating principles.

A. Case 1: Transformer Design of LLC

Magnetics design is crucial for transformer-based topologies. As the manufacturing technology of emerging wide-bandgap semiconductors such as Gallium Nitride (GaN) gradually matures, the switching frequency can be pushed to several MHz to reduce the size of the transformer. However, the winding losses of conventional wire-wound magnetic components limit the power density and efficiency due to the eddy current loss in round conductors, particularly at frequency above 100 kHz [55]. To resolve this issue, integrated planar magnetics with PCB winding and matrix transformer has been investigated to optimize the high-frequency transformer [21], [22], [27], [28], [56], [57]. In 48 V data center VRMs, the high voltage conversion ratio and high output current need a large turn ratio of the transformer. For instance, the *LLC* DCX used in Sigma structure [28] has a 40-to-1 turns ratio which utilizes four discrete 10-to-1 transformers to handle the high turns ratio and high current. The schematic of the *LLC* DCX is illustrated in Fig. 18. Multiple transformers with separate magnetic cores increase the footprint and core loss. Correspondingly, the optimized single matrix transformer integrates the four transformers into one core structure and merges the center leg as the return flux path of each elemental transformer. Since the flux in the center leg can cancel each other by arranging the current direction of four elemental transformers, removing this

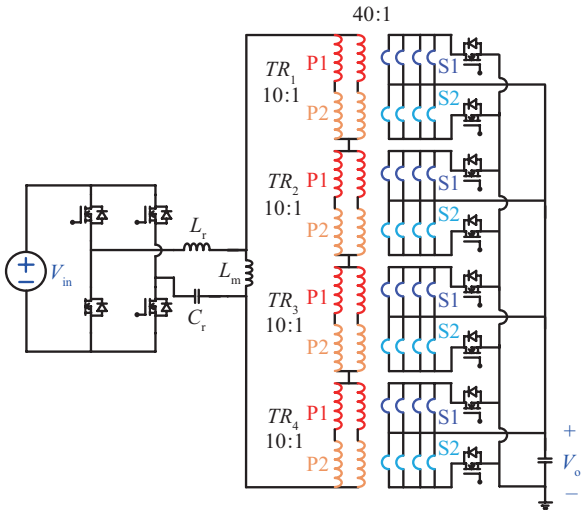

Fig. 18. 40-to-1 *LLC* DCX with matrix transformer [28].

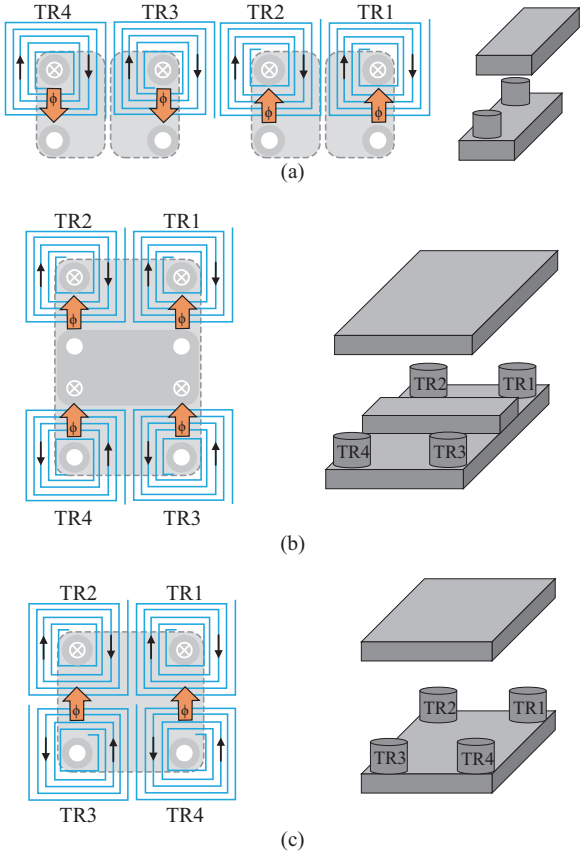

Fig. 19. Derivation of the matrix transformer [28]: (a) original four elemental transformer structure with separate UI-cores; (b) rearranged four elemental transformers integrated in one core with a wide center leg; (c) integrated matrix transformers with one core structure without center leg.

center leg will reduce total core losses without scarifying any winding. The derivation of the proposed matrix transformer is shown in Fig. 19. Moreover, the single-core ensures a symmetrical air gap which facilitates the current balance.

Another optimized aspect of the matrix transformer is the winding arrangement. Fig. 20 shows the detailed PCB winding

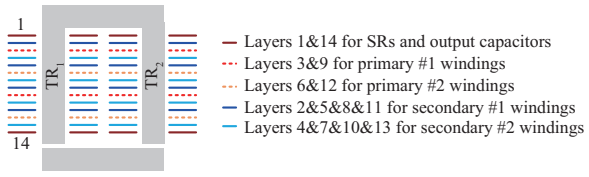

Fig. 20. 14 layers PCB winding arrangement [28].

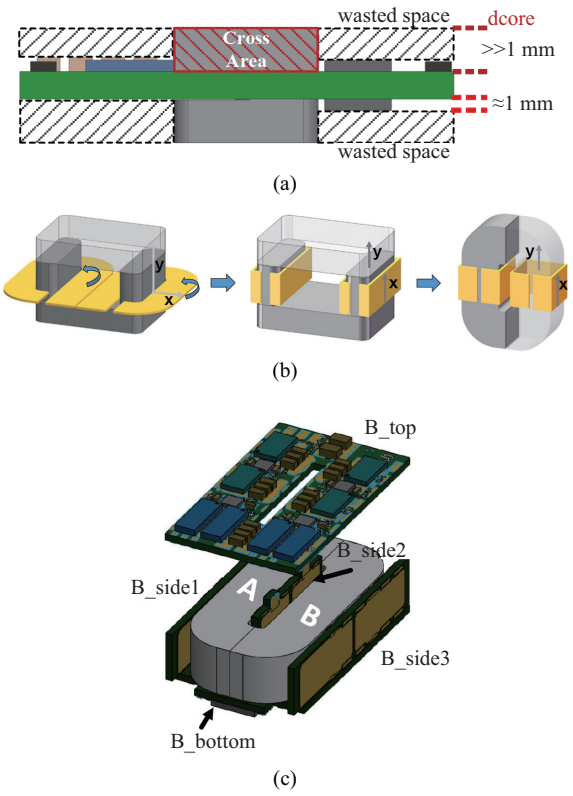

Fig. 21. (a) Conventional Planar PCB *LLC* DCX; (b) Optimized parallel PCB windings; (c) Exploded view of the 3D PCB winding transformer [58].

arrangement of the transformer in Fig. 18, and the windings correspond to each other by color. Multiple sets of primary or secondary windings are paralleled to reduce conduction losses, and the interleaved arrangement of the primary and secondary windings can significantly reduce the ac losses caused by the proximity effect.

Although the planar transformer with PCB windings has a low profile, the thickness of the magnetic core is still far higher than that of other devices. This results in wasted space as shown in Fig. 21(a). To efficiently exploit the wasted vertical space and to improve the limited power density of the conventional planar transformer, a 3D PCB winding structure is proposed in [58] and the optimized parallel PCB windings are illustrated in Fig. 21(b). It uses the parallel PCB as the winding to tightly surround the magnetic core and mounts all components on the top and bottom layers of the PCB. Hence, the wasted space caused by mismatched component thicknesses can be greatly reduced, and the exploded view of the 3D PCB winding transformer is illustrated in Fig. 21(c). In addition, the width of parallel PCB windings is significantly increased to carry a

higher current.

In conclusion, the magnetic core and winding arrangement of the matrix transformer is the key to magnetics design.

B. Case 2: Resonant Component Selection of STC

For ZCS-type STC as shown in Fig. 10, all the resonant tanks are considered to have matched resonant frequency since the resonant components of all resonant tanks are identical. Therefore, the proposed converter can achieve ZCS as long as the switching frequency is matched to the resonant frequency. However, practically, once there is a minor mismatch in the resonant parameters, ZCS will be lost. Many factors can cause the mismatch of the resonant parameters in different resonant loops such as the tolerance of resonant components and the PCB parasitic components. For the capacitor design, Fig. 22 presents the capacitance change of two 50 V capacitors with the dc-bias voltage, and it is obvious that the dielectric material determines the stability of capacitance. Table VI [7] compares the features of class I (U2J, C0G) and II (X5R, X7R) capacitors. Therefore, the capacitor with class I material can be used as the resonant capacitor which has rigid requirements on capacitance accuracy, and the non-resonant flying capacitor can select the capacitor with class II material with better volume efficiency to increase the capacitance.

For the STC inductor design, the inductors in the resonant tanks can utilize the PCB parasitic inductors as mentioned in Section V-A, and the equivalent circuit is shown in Fig. 23. Although the required inductance is small (~nH), the thickness of the discrete inductor core is much higher than the other devices such as MOSFETs and ceramic capacitors. This leads to wasted space which decreases power density [59]. An empirical formula in [60] to calculate parasitic inductance of PCB copper traces is expressed as (2).

$$L = 2l \times (\ln \frac{2l}{w} + 0.5 + 0.2235 \frac{w}{l}) \tag{2}$$

where l, w are the length and the width of PCB trace, respectively.

To obtain enough inductance, the PCB trace will be very long since the PCB parasitic inductance is usually small, which affects the power density. Coupled inductance is a method to increase the parasitic inductance values, and the coupling coefficient depends on the winding layout. The vertical structure has a better coupling coefficient than the lateral structure and the effective area of the high-frequency current is larger since the width of the copper layer is much larger than its thickness in the vertical structure. Therefore, the vertical structure of PCB winding can efficiently use the PCB parasitic inductance to improve the power density. The detailed analysis and results are depicted in [59].

VIII. Opportunities and Challenges

With the product and technology iteration, the terminal load CPU/GPU current demand has been increasing year by year, while the core voltage has decreased to sub-volt. Thus, the applications of low voltage and high current are becoming increasingly important. It brings both challenges and opportunities to the development of data center power technologies.

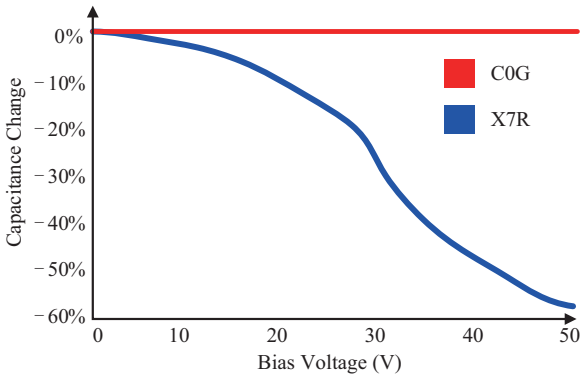

Fig. 22. The capacitance changes of different class 50 V capacitors versus dc-bias voltage.

TABLE VI
Resonant Capacitor Comparison [7]

Capacitor Class	Capacitor Drop with dc Bias	Stability	Volume Efficiency
Class I (U2J, C0G)	<1%	Exceptional	Good
Class II (X5R, X7R)	Large Drop	Good	Exceptional

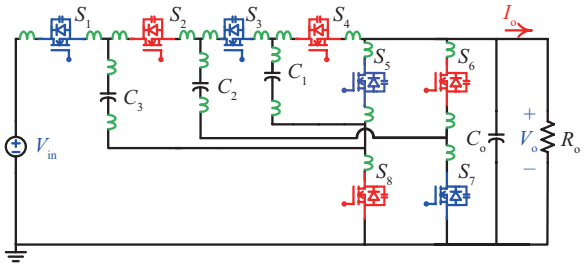

Fig. 23. The equivalent circuit of STC in Fig. 10 with parasitic inductors.

The first opportunity and challenge is single-stage VRM for 48 V bus power system. Although the two-stage structure still dominates the market due to its good deployment flexibility and transient performance, and reuse of traditional 12 V power systems. However, the single-stage structure has the potential to achieve higher conversion efficiency and power density. The major constraint of the single-stage is the high voltage conversion ratio. On the one hand, the inductive single-stage structure solution generally utilizes a transformer with a large turns ratio to achieve a high step-down ratio, which is also critical to the optimal design of the transformer. On the other hand, the hybrid SCCs handle this issue based on modular expansion, so a large number of components are required and there may be troubles in module balance. Therefore, no matter which solution is adopted, implementing a highly integrated topology and a simple control method can better take

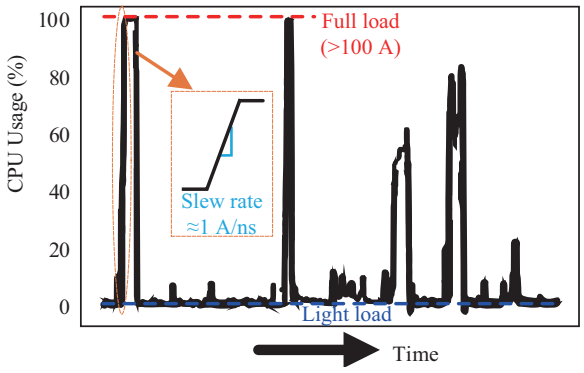

Fig. 24. The CPU usage status versus time [63], [64].

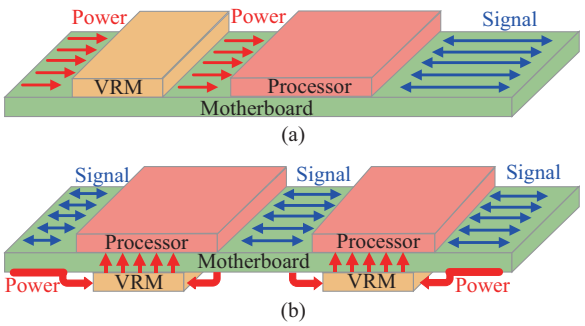

Fig. 25. Power delivery architecture [46]: (a) Conventional lateral power delivery; (b) Vertical power delivery.

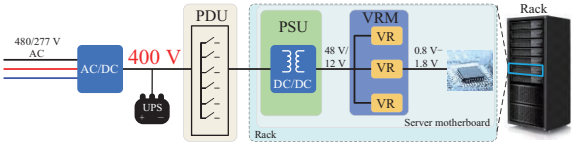

Fig. 26. Future architecture with 400 V bus [56], [77].

advantage of the single-stage structure, and the single-stage will become a mainstream solution in the future.

Another opportunity and challenge is the dynamic response of PoL converter. The terminal loads mainly operate under standby (idle) and light-load conditions [61]. Thus, extremely high di/dt (up to 1000 A/μs) [62] (as shown in Fig. 24 [63], [64]) is inevitable during the load transition to meet the ultrahigh current requirements. Meanwhile, PoL converters must maintain stable output voltage regulation with high efficiency over a large dynamic load range. Increasing the output filter capacitance is a direct and effective method to suppress transient perturbations, but this sacrifices power density. To optimize the bulky output capacitors, VRMs should be responsible for supplying instantaneous large current change demand. This requires VRMs to have fast transient response performance, and "fast" means that response is typically within one or two switching periods [65]. Hence, high switching frequency and high bandwidth are beneficial to facilitate response speed. Constant on-time (COT) control [66] is a popular variable-frequency control technique to address this transient response issue in PoL converters due to its better light-load efficiency and high-bandwidth design capability. However, the transient response of conventional COT control is limited by the fixed on-time, and this may result in large output voltage undershoot or overshoot at an extreme current slew rate. Consequently, some adaptive COT-based techniques are proposed [64], [67]–[69] to further improve the transient performance. Furthermore, time-optimal control with a single-cycle response [70]–[72] can achieve the best transient performance due to the minimum voltage perturbation and settling time. For instance, [73] proposes a state-trajectory-based control with single-cycle response to achieve a seamless transition between steady-state and transient-state, and the converters can ensure a very fast transient response. Alternatively, smaller output inductance also responds promptly to load transients, but a large peak-peak current ripple will be induced with more switching losses and ac conduction losses [74]. Correspondingly, a topology optimization named trans-inductor voltage regulator (TLVR) [75], [76] is proposed to address this tradeoff without extra control. It is derived based on a multi-phase converter with coupled inductors, and the equivalent transient inductance can be reduced during load transients. Compared with traditional multi-phase coupled, it introduces additional compensation inductance to induce the current changes of each phase. This significantly improves the scalability and integration in practical industrial manufacturing. TLVR technology unblocks the long-standing theoretical bandwidth barrier and improves transient performance without sacrificing steady-state performance. Moreover, it should be mentioned that TLVR is topology-level innovation that can be compatible with most traditional control methods. Nevertheless, the above-mentioned methods for dynamic response are generally suitable for multi-phase buck converters, so there are still many potential optimization issues in improving the transient performance of various VRMs in data center applications.

In addition to the improvement of topology and control, the advantages of vertical power delivery structure are emerging as the power scales up. Fig. 25(a) shows the conventional lateral power architecture on the server motherboard, and a large part of the area is occupied for power transmission. This results in heavy ineffective losses due to the ultrahigh current near the terminal loads. Therefore, direct vertical power delivery with VRM mounted on the surface of terminal loads can significantly reduce the power transmission path, thereby supporting higher power levels and achieving higher efficiency. The vertical power delivery architecture is shown in Fig. 25(b). At present, there have been VRMs with 3D structure for vertical power delivery [46]–[48]. Thanks to the reduced losses in the transmission path, the current supported by a single VRM can reach 780 A with 91.1% peak efficiency and 1 A/mm^2 current density [48]. However, to be better mounted on the load surface, the thickness requirements of the vertical structure must also be strict. Thus, the tradeoff between the thickness and vertical structure is also the focus of future optimization in data center power systems.

Besides, many other opportunities and challenges such as

higher bus voltage (eg. 400 V as shown in Fig. 26 [56], [77]) are also important for optimizing the power system in data center.

IX. Conclusions

The new generation 48 V bus power system in data center poses significant challenges in the design of 48 V VRMs with high conversion efficiency, high power density and low cost. This paper gives an overview of 48 V VRMs and divides them into inductive and capacitive categories according to the type of passive components. The inductive solution can be further divided into the coupled-inductor-based converters and transformer-based converters, while the capacitive-based solution can also be further divided into Resonant SCC and Hybrid SCC. The performances of the corresponding converters are briefed and compared, and some design considerations are analyzed as the case study to take into account the tradeoffs when designing the practical prototypes. Moreover, the opportunities and challenges provide an outlook for future data center power system research. Therefore, further research based on the current power system may greatly address the current limitations to enable more efficient and greener data center energy utilization.

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Jiawei Liang received the bachelor's degree in electronic information engineering from Shanghaitech University, Shanghai, China, in 2020. He is currently working toward the master's degree in electrical engineering with the School of Information Science and Technology, Shanghaitech University, Shanghai, China.

His current research interests include switched-capacitor converter, point-of-load converter, and magnetic integration in data center applications.

Liang Wang received the B.S. degree in electrical engineering and automation from Harbin Engineering University, Harbin, China, in 2019. He is currently working toward the Ph.D. degree with the School of Information Science and Technology, ShanghaiTech University, Shanghai, China.

His research interests include renewable energy systems, multiport converters, and energy harvesting systems.

Minfan Fu received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from the University of MichiganShanghai Jiao Tong University Joint Institute, Shanghai Jiao Tong University, Shanghai, China, in 2010, 2013, and 2016, respectively. From 2016 to 2018, he was a Postdoctoral with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. He is currently an Assistant Professor with the School of Information Science and Technology, ShanghaiTech University, Shanghai, China. He holds one U.S. patent, three Chinese patents, and has authored or coauthored more than 50 papers in prestigious IEEE journals and conferences.

His research interests include megahertz wireless power transfer, high-frequency power conversion, high-frequency magnetic design, and application of wide-bandgap devices.

Junrui Liang received the B.E. and M.E. degrees in instrumentation engineering from Shanghai Jiao Tong University, Shanghai, China, in 2004 and 2007, respectively, and the Ph.D. degree in mechanical and automation engineering from The Chinese University Hong Kong, Hong Kong, in 2010. He is currently an Associate Professor with the School of Information Science and Technology, ShanghaiTech University, Shanghai, China.

His research interests include energy conversion and power conditioning circuits, kinetic energy harvesting and vibration suppression, IoT devices, and mechatronics.

Haoyu Wang received the bachelor's degree (with Distinguished Hons.) in electrical engineering from Zhejiang University, Hangzhou, China, in 2009, and the Ph.D. degree in electrical engineering from the University of Maryland at College Park, College Park, MD, USA, in 2014. In September 2014, he was with the School of Information Science and Technology, ShanghaiTech University, Shanghai, China, where he is currently a tenured Associate Professor.

His research interests include power electronics, plug-in electric and hybrid electric vehicles, the applications of wide-bandgap semiconductors, renewable energy harvesting, and power management integrated circuits.

Dr. Wang is an Associate Editor for the *IEEE Transactions on Industrial Electronics, IEEE Transactions on Transportation Electrification,* and *CPSS Transactions on Power Electronics and Applications.*