# A Merged H-Bridge Based Switched Tank Converter for Front-End Voltage Regulator Modules 

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#### Abstract

In this paper, a merged H-bridge based switched tank converter is proposed to serve as the front end nonregulated stage of voltage regulator modules. To achieve an $n: 1$ voltage step down ratio, only $n+4$ switches are required. The proposed converter maintains good soft-charging and softswitching performances, which effectively mitigate the switching loss. No bulky transformer is required. The design considerations of the tolerance of resonant components is also presented. A small deadband and symmetrical printed-circuit-board design are dedicated to compensating the deviation of resonant frequency caused by tolerance in resonant components. Zero current switching is achieved among all MOSFETs. The low switch count and zero current switching performance facilitate both high power density and high efficiency of the designed prototype. Steady-state circuit analysis is briefed and the simulation model is established to verify the analysis. To verify the proposed concept, a hardware prototype that converts 48 V to 8 V is designed and tested. The maximum output current can reach 28 A , and the peak efficiency is $\mathbf{9 7 . 1 1 \%}$ at 6.2 A output.


Index Terms-switched-tank converter, high efficiency, resonant, soft-charging, zero current switching.

## I. Introduction

Nowadays, emerging information technologies such as 5G communication, big data, and artificial intelligence are boosting a fast-growing power consumption in data centers [1]. In data centers, terminal loads such as memory and computing units operate at a very low logic voltage ( $1 \mathrm{~V}-1.8 \mathrm{~V}$ ), which makes it challenging to optimize the design of the load side voltage-regular-modules (VRM). For the VRM, a popular power architecture is 48 V distribution bus-based two-stage structure. A non-regulated converter is utilized in the front end to convert the 48 V to an intermediate voltage (e.g. 5 $\mathrm{V}-12 \mathrm{~V}$ ), and a point-of-load ( PoL ) converter is employed in the back end to regulate the intermediate voltage to $1 \mathrm{~V}-1.8 \mathrm{~V}$ for terminal loads. For the front-end non-regulated converters, high conversion efficiency, high power density, and low cost are the major desired features.

In the front end, full bridge LLC resonant converter [2] is a popular candidate due to its zero-voltage-switching (ZVS) for primary side MOSFETs and zero-current-switching (ZCS) for secondary side diodes. However, at light load, a large circulating current in the LLC transformer degrades the conversion

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efficiency. Moreover, the LLC transformer is bulky, which degrades the power density. As an alternative, switched capacitor converter (SCC) based solutions are proposed [3]-[6]. In SCC, only capacitors are employed to transfer energy; the magnetic components are eliminated. Hence, the power density can be effectively enhanced. However, harsh transient currents might occur when the capacitors are reconfigured, which leads to severe charge redistribution loss. Correspondingly, small inductors can be inserted into SCC to better shape the transient currents. In [7], a switched-tank converter (STC) is proposed to serve as the front stage non-regulated converter. In STC, small inductors resonate with the corresponding capacitors, which facilitates a soft charging of capacitors. ZCS of all MOSFETs is achieved, which effectively reduces the device switching loss. However, to achieve an $n: 1$ voltage step-down ratio, $3 n$ 2 MOSFETs are required. The high MOSFETs count leads to both increased cost and large circuit size.

To improve, this paper proposes a new switched tank converter for front-end VRMs. Different conversion ratios can be achieved by customizing the wing-side switch networks. With different wing-side switch networks, the bridge side always utilizes a fixed H bridge structure. This converter can operate under ZCS, which is more beneficial than ZVS in high current applications. Compared with conventional STC converter, the merged H bridge based STC converter can achieve the same conversion ratio with a much lower switch count. This helps reduces the power loss, material cost, and circuit size. Basic converter operation is analyzed and the simulation of the proposed merged H bridge-based STC converter has been carried out to verify the concept. A 48 V -to- 8 V , fixed ratio converter prototype is built and tested to verify the theoretical analysis.

The rest of the paper is organized as follows. Section II introduces the proposed converter along with its steady-state operation and presents the steady-state analysis of important waveforms in a design-oriented manner. In Section III, the simulation model of the proposed converter is carried out with Simulink platform. Moreover, a 48 V input to $8 \mathrm{~V} / 28$ A output hardware prototype is developed and the experimental results are demonstrated. Finally, the conclusion is given in Section IV.


Fig. 1. Schematic of the proposed 6-to-1 STC Converter based on merged H-bridge.


Fig. 2. Idealized switching waveforms.

## II. Operation Principle and Analysis

## A. Proposed Converter and Operating Principle

Fig. 1 shows the schematic of the proposed converter with 6:1 conversion ratio. The proposed STC converter can be derived from the typical 6:1 STC converter reported in [8] by merging five half bridges on the bridge side into one H bridge. Generally, an STC converter with an $n: 1$ conversion ratio requires $n$ switches on the wing side and $2 n-2$ switches on the bridge side [8]. However, on the bridge side, multiple branch currents share the same direction and one common convergence point. This means one H -bridge is sufficient to achieve the same operating modes without affecting circuit performance. Therefore, the proposed converter can achieve the same conversion ratio with much fewer switches, which facilitates higher power density and lower switching loss.

The circuit operation can be divided into two modes. All the switches can be divided into two groups, which are odd (blue) group and even (red) group. Switches with identical color are driven by the same PWM signal. Two $50 \%$ duty cycle complementary PWM signals with certain deadband are utilized to drive all the switches. The key waveforms of

TABLE I
Voltage Rating Comparison

| Topology | Switch Count | Voltage Stress |
| :---: | :---: | :---: |
|  |  | $5 V_{o}(3$ MOSFETs $)$ <br> $4 V_{o}(2$ MOSFETs $)$ |
| Series-Parallel | 16 | $3 V_{o}(2$ MOSFETs $)$ <br> $2 V_{o}(2$ MOSFETs $)$ <br> $V_{o}(7$ MOSFETs $)$ |
| STC [7] | 16 | $2 V_{o}(4$ MOSFETs $)$ <br> $V_{o}(12$ MOSFETs $)$ |
| Multi-Resonant SCC [9] | 10 | $3 V_{o}(4$ MOSFETs $)$ <br> $2 V_{o}(2$ MOSFETs $)$ <br> $V_{o}(4$ MOSFETs $)$ |
| Proposed | 10 | $2 V_{o}(4$ MOSFETs) <br> $V_{o}(6$ MOSFETs $)$ |

gate signals switch currents and voltages, inductor currents, and capacitor voltages are illustrated in Fig. 2. The operation modes neglecting the dead time are analyzed as follows:

1) Mode $I\left(t_{0}-t_{1}\right)$ : Odd (blue) switches are on, even (red) switches are off, input voltage source $V_{\text {in }}$ charges resonant capacitor $C_{5}$ and $C_{\text {out }}$, non-resonant capacitor $C_{4}$ charges $C_{3}$ and $C_{\text {out }}$ and $C_{2}$ charges $C_{1}$ and $C_{\text {out }}$.
2) Mode II $\left(t_{1}-t_{2}\right)$ : Even (red) switches are on, odd (blue) switches are off, resonant capacitor $C_{5}$ charges non-resonant capacitor $C_{4}$ and $C_{o u t}, C_{3}$ charges $C_{2}$ and $C_{o u t}$, and $C_{1}$ charges $C_{\text {out }}$.

When the switching period is over, the resonant current reaches zero. The switching frequency is equal to resonant frequency so that the switching transition and resonant current are in phase. This ensures a zero current switching with reduced switching loss,

$$
\begin{equation*}
f_{s}=f_{r}=\frac{1}{2 \pi \sqrt{L_{r} C_{r}}} \tag{1}
\end{equation*}
$$

where $f_{s}, f_{r}, L_{r}$, and $C_{r}$ are the switching frequency, resonant frequency, resonant inductance, and resonant capacitance in the resonant tank, respectively.

## B. Electrical Rating Comparison

The capacitor voltages satisfy $V_{n}=n V_{o}(n=1,2, \ldots, 5)$. The voltage stresses of the switches $S_{1}, S_{6-10}$ are $V_{o}$ and the switches $S_{2-5}$ have the voltage stress $2 V_{o}$.
The voltage stresses of switches among various 6:1 hybrid/resonant switched-capacitor converter (SCC) topologies are compared. Table I indicates that the proposed converter has the lowest voltage stress.

## C. Resonant Tank Design Considerations

For the proposed STC converter, designing the parameters of the resonant tank is very critical. To select proper resonant inductance and capacitance, the waveforms of the current and voltage for inductors and capacitors should be analyzed. The equivalent circuits are shown in Fig. 3. The resonant inductor current $i_{L r}(t)$ can be derived,

$$
\begin{equation*}
i_{L r}(t)=I_{\text {peak }} \sin \left(\omega_{r} t\right)=\frac{\pi}{6} I_{o} \sin \left(\omega_{r} t\right)=\frac{\pi P_{o}}{6 V_{o}} \sin \left(\omega_{r} t\right) \tag{2}
\end{equation*}
$$



Fig. 3. Equivalent circuits of the proposed converter: (a) Mode I; (b) Mode II.

Then the voltage of the resonant capacitor $v_{C n}(t)$ ( $n=$ $1,3,5$ ) can be calculated by solving the following differential equations,

$$
\begin{align*}
& \left\{\begin{array}{l}
v_{C n}(t)+L_{r} \frac{d i_{L r}(t)}{d t}=n V_{o} \\
i_{L r}(t)=i_{C n}(t)=C_{n} \frac{d v_{C n}(t)}{d t}
\end{array}\right.  \tag{3}\\
\Rightarrow & \left\{\begin{array}{l}
v_{C n}(t)=n V_{o}-\frac{\pi \omega_{r} L_{r} P_{o}}{6 V_{o}} \cos \left(\omega_{r} t\right) \\
\Delta v_{C n}=\frac{2 \pi \omega_{r} L_{r} P_{o}}{6 V_{o}}
\end{array}\right. \tag{4}
\end{align*}
$$

where $n V_{o}$ is the average voltage across the $n^{t h}$ resonant capacitor. The resonant inductor current and capacitor voltage expressions show that the inductor current and capacitor voltage ripples are affected by resonant inductance, resonant frequency, and output power.

## D. Tolerance of Resonant Components

In the theoretical analysis, all the resonant tanks are considered to have the same resonant frequency since the resonant


Fig. 4. The resonant periods considering the tolerance of resonant components.
components of all resonant tanks are identical. Therefore, the proposed converter can achieve ZCS as long as the switching frequency is matched to the resonant frequecny. However, in practice, once there is a small error in the resonant parameters, ZCS will be lost. There are many factors that can cause the mismatch of the resonant parameters in different resonant loops. Firstly, it is not easy to ensure that all of the resonance capacitors and inductors have identical values. Even if the manufacturer has strict quality control and advanced manufacturing processes, the tolerance of capacitors and inductors still can not be ignored. Secondly, the parasitic components such as printed-circuit-board (PCB) inductors may also change the resonant parameters in the loop. The above two factors affect the resonant frequency, which causes the loss of ZCS operation and increases the loss. Specially, the ZCS-type SCC converter must be designed to handle this tolerance in massive production. Some references [8], [10] have mentioned this problem, and the general method is to add a deadband during the switching transition to reset all inductor currents. In order to calculate the dead time, it is assumed that the resonant inductance and capacitance are both around the nominal value $\pm 5 \%$. Fig. 4 shows the waveforms of the minimum resonant period, the nominal resonant period, and the maximum resonant period. Then, the minimum deadtime $t_{d, \text { min }}$ can be estimated as,

$$
\begin{align*}
t_{d, \min } & =\frac{1}{2}\left(T_{\max }-T\right)=\pi \sqrt{L_{r, \max } C_{r, \max }}-\pi \sqrt{L_{r} C_{r}} \\
& =(1+5 \%) \pi \sqrt{L_{r} C_{r}}-\pi \sqrt{L_{r} C_{r}}=5 \% \pi \sqrt{L_{r} C_{r}} \\
& =2.5 \% T \tag{5}
\end{align*}
$$

where $T$ and $T_{\max }$ are the nominal resonant period and the maximum resonant period, respectively.

Furthermore, the symmetrical PCB design of all resonant loops are also essential to minimize the influence of parasitic parameters.

## E. Power Loss Analysis

The power loss is an important consideration in selecting suitable components and designing the PCB. Moreover, lower
power loss means higher conversion efficiency which is a vital figure of merit to evaluate the performance of the converter. As shown in Eq. (6), the total power loss includes the gate drive loss, conduction loss and switching loss of the MOSFETs, conduction loss of the capacitors and inductors, and PCB loss.

$$
\left\{\begin{array}{l}
P_{l o s s}=P_{m o s}+P_{c a p}+P_{\text {inductor }}+P_{p c b}  \tag{6}\\
P_{\text {mos }}=P_{g a t e}+P_{c o n d}+P_{s w}
\end{array}\right.
$$

Typically, the gate drive loss of MOSFETs can be estimated as,

$$
\begin{equation*}
P_{\text {gate }}=V_{g s} Q_{g} f_{s} \tag{7}
\end{equation*}
$$

where $V_{g s}$ is drive voltage of MOSFETs, $Q_{g}$ is the gate charge of MOSFETs, and $f_{s}$ is the switching frequency. The conduction loss of MOSFETs can be calculated using Eq. (8).

$$
\begin{equation*}
P_{\text {cond }}=I_{r m s}^{2} R_{o n} \tag{8}
\end{equation*}
$$

where $R_{o n}$ is the on-resistance of the MOSFETs. Since all of the switches operate with ZCS, the switching loss is caused by the output capacitor. When the MOSFETs is off, the output capacitor of MOSFETs will be charged, and these charges will be dissipated within the MOSFETs when the MOSFETs turn on. Thus, the switching loss can be expressed as,

$$
\begin{equation*}
P_{s w}=C_{o s s} V_{d s} f_{s} \tag{9}
\end{equation*}
$$

where $C_{o s s}$ and $V_{d s}$ are the output capacitance and the drain-to-source voltage of MOSFETs, respectively.

The power loss of capacitors and inductors is mainly the conduction loss due to their equivalent series resistance (ESR). The ESR of capacitor can be reduced by parallelling multiple small capacitors. The PCB power loss distribution and estimation can be carried out via finite-element-analysis (FEA) software.

## III. Simulation and Experimental Results

## A. Simulation Results

In order to validate the operating principle, the proposed converter with a $6: 1$ conversion ratio is simulated in Simulink. The key parameters are listed in Table II. Fig. 5 shows the simulation results of the proposed converter. The voltage stresses of MOSFETs are $8 \mathrm{~V}\left(S_{1,6-10}\right)$ and $16 \mathrm{~V}\left(S_{2-5}\right)$, respectively. The current stresses of MOSFETs are 13 A $\left(S_{1-6}\right), 26 \mathrm{~A}\left(S_{8,9}\right)$, and $39 \mathrm{~A}\left(S_{7,10}\right)$, respectively. The average voltages of capacitors $C_{1-5}$ are $8 \mathrm{~V}, 16 \mathrm{~V}, 24 \mathrm{~V}, 32$ V , and 40 V , respectively. When the switching frequency is close to the resonant frequency, the resonant current reaches zero at the switch transitions which means the switches can achieve ZCS operation.

## B. Experimental Results

A hardware prototype based on the proposed concept has been built to verify the $6: 1$ conversion ratio and ZCS operation. Its top and bottom views can be found in Fig. 6. The main power circuit, gate driver circuit and isolated power circuit are all installed on the main PCB. The dimension of the

TABLE II
Parameters of Proposed Converter

| Names | Values |
| :---: | :---: |
| Input Voltage $V_{i n}$ | 48 V |
| Output Voltage $V_{o}$ | 8 V |
| Resonant Capacitor $C_{r}$ | $1.76 \mu \mathrm{~F}$ |
| Non-Resonant Capacitor $C_{n r}$ | $100 \mu \mathrm{~F}$ |
| Resonant Inductor $L_{r}$ | 200 nH |
| Resonant Frequency $f_{r}$ | 268 kHz |
| Switching Frequency $f_{s}$ | 255 kHz |
| Load $R_{\text {load }}$ | $0.3 \Omega$ |


(a)

(b)

Fig. 5. Simulation results: (a) voltage/current waveforms of switches and current waveforms of inductors; (b) voltage waveforms of capacitors.
prototype is $3.26 \times 3.23 \times 0.67 \mathrm{in}^{3}$, and the main power area size is $2.56 \times 1.82 \times 0.54 \mathrm{in}^{3}$. The components used in this prototype are listed in Table III. DSP TMS320F28379 is used as the digital controller to generate the pulsewidth modulation signals. The prototype operates at $255 \mathrm{kHz}, 48 \mathrm{~V}$ input and $8 \mathrm{~V} / 28$ A output with a 100 ns dead time. The experimental


Fig. 6. Picture of the designed prototype: (a) top view; (b) bottom view.

TABLE III
Components of Prototype

| Components | Part number |
| :---: | :---: |
| MOSFET | BSZ013NE2LS5I (25 V, 1.3 m $)$ |
| Resonant Capacitor | C1812C224J5GAC |
| Non-Resonant Capacitor | CGA6P1X7R1N106M250AC |
| Resonant Inductor | SLC7649S-101KLC |
| Gate Driver | LM5113SD |
| Digital Isolator | Si8620BB |
| Isolated Power | B0505XT-1WR3 |

results are captured in Fig. 7-10. Fig. 7 shows the current waveforms of three resonant inductors. All current waveforms are almost identical due to 1) each resonant tank adopts identical resonant parameters; and 2) the current loops in the PCB layout are highly symmetrical. The resonant capacitor voltage waveforms are shown in Fig. 8. The ripple voltages of three resonant capacitors are nearly identical. The nonresonant capacitor voltages can be considered as dc voltage, and the measured input voltage and output voltage exhibit a 6:1 conversion ratio, as shown in Fig. 9. To demostrate ZCS operation intuitively, the scaled resonant inductor current and gate drive signal are illustrated in Fig. 10. The resonant current reaches zero at the switch transition point which indicates ZCS operation is achieved.

The conversion efficiency of the designed prototype is evaluated in different output currents at 255 kHz switching


Fig. 7. Current waveforms of resonant inductors.


Fig. 8. Voltage waveforms of resonant capacitors.


Fig. 9. Voltage waveforms of input voltage, output voltage and non-resonant capacitors.
frequency. Fig. 11 shows the efficiency curve versus output current. When the output current is small, the fixed power loss such as switching loss dominates the total loss. As the output current increases, the efficiency gradually improves. When the output current increases to $6.2 \mathrm{~A}, 97.11 \%$ peak efficiency is captured. Then, the total loss is mainly composed of conduction loss caused by the equivalent series resistance


Fig. 10. ZCS waveforms of the designed prototype.


Fig. 11. Measured efficiency versus output current.

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of the loops. The efficiency begins to decrease as the output current increases.

## IV. Conclusions

In this paper, a merged H -bridge based STC converter is proposed for front-end VRMs. It can achieve the same conversion ratio as conventional STC converter or other resonant switched-capacitor converters with fewer switches, thereby improving power density and efficiency. The proposed converter provides several advantages including: a) all the MOSFETs operate with ZCS which is more beneficial than ZVS in high current applications; b) fewer switches lead to higher power density and lower switching loss; c) easy open-loop control with a pair of $50 \%$ duty cycle complementary gate signals. The simulation and experimental results are presented to validate the analysis. Moreover, a small deadband and sysmmetrical PCB design make all the MOSFETs operate with ZCS to reduce the switching loss. A 48 V input to $8 \mathrm{~V} / 28$ A output hardware prototype is designed and tested. The peak efficiency is $97.11 \%$ at 6.2 A output. In the future, a more compact converter prototype with smaller parasitic parameters and more layers of PCB will be designed to further improve efficiency and power density.

